Open-Q™ 670 HDK Hardware Development Kit User Guide

[Document: ITC-01CGS1394-UG-001 Version: 1.0]

IDENTIFICATION

Document Title	Open-Q™ 670 HDK Hardware Development Kit User Guide
Document Number	ITC-01CGS1394-UG-001
Version	1.0
Date	December 10, 2018

Revision History

REVISION	DATE	DESCRIPTION	PAGES
1.0	December 10, 2018	Initial Draft, from 80-PJ602-2_B_HDK670(SDA670)	All

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1. INTRODUCTION

1.1 Purpose

The purpose of this user guide is to provide primary technical information on the Open-Q™ 670 HDK Hardware Development Kit.

For more background information on this development kit, visit: www.intrinsyc.com

1.2 Scope

This document will cover the following items on the Open-Q 670 Hardware Development Kit:

- Block Diagram and Overview
- Hardware Features
- Configuration
- Processor board
- Carrier Board
- Display Board for LCD

1.3 Intended Audience

This document is intended for users who would like to develop custom applications on the Intrinsyc Open-Q 670 Hardware Development Kit.

2. DOCUMENTS

This section lists the supplementary documents for the Open-Q 670 Hardware Development Kit.

2.1 Applicable Documents

REFERENCE	TITLE
A-1	Intrinsyc Purchase and Software License Agreement for the Open-Q Development Kit

2.2 Reference Documents

REFERENCE	TITLE

2.3 Terms and Acronyms

Term and acronyms	Definition
AMIC	Analog Microphone
ANC	Audio Noise Cancellation
B2B	Board to Board
BLSP	Bus access manager Low Speed Peripheral (Serial interfaces like UART / SPI / I2C/ UIM)
BT LE	Bluetooth Low Energy
CSI	Camera Serial Interface
DSI	MIPI Display Serial Interface
EEPROM	Electrically Erasable Programmable Read only memory
eMMC	Embedded Multimedia Card
FCC	US Federal Communications Commission
FWVGA	Full Wide Video Graphics Array
GPS	Global Positioning system
HDMI	High Definition Media Interface
HSIC	High Speed Inter Connect Bus
JTAG	Joint Test Action Group
LNA	Low Noise Amplifier
MIPI	Mobile Industry processor interface
MPP	Multi-Purpose Pin
NFC	Near Field Communication
RF	Radio Frequency
SATA	Serial ATA
SLIMBUS	Serial Low-power Inter-chip Media Bus
SPMI	System Power Management Interface (Qualcomm® PMIC / baseband proprietary protocol)
SSBI	Single wire serial bus interface (Qualcomm® proprietary mostly PMIC / Companion chip and baseband processor protocol)
UART	Universal Asynchronous Receiver Transmitter
UFS	Universal Flash Storage
UIM	User Identity module
USB	Universal Serial Bus
USB HS	USB High Speed
USB SS	USB Super Speed

2.4 List of Figures

2.5 List of Tables

3. OPEN-Q 670 HARDWARE DEVELOPMENT KIT

3.1 Introduction

The Open-Q 670 Hardware Development Kit provides a quick reference or evaluation platform for Qualcomm's Snapdragon™ SDA670 processor. This kit is suited for Android / Linux application developers, OEMs, consumer manufacturers, hardware component vendors, video surveillance, robotics, camera vendors, and flash chip vendors to evaluate, optimize, test and deploy applications that can utilize the Qualcomm® Snapdragon™ 670 series technology.

3.2 Development Platform Notice

This development platform contains RF/digital hardware and software intended for engineering development, engineering evaluation, or demonstration purposes only and is meant for use in a controlled environment. This device is not being placed on the market, leased or sold for use in a residential environment or for use by the general public as an end user device.

This development platform is not intended to meet the requirements of a commercially available consumer device including those requirements specified in the European Union directives applicable for Radio devices being placed on the market, FCC equipment authorization rules or other regulations pertaining to consumer devices being placed on the market for use by the general public.

This development platform may only be used in a controlled user environment where operators have obtained the necessary regulatory approvals for experimentation using a radio device and have appropriate technical training. The device may not be used by members of the general population or other individuals that have not been instructed on methods for conducting controlled experiments and taking necessary precautions for preventing harmful interference and minimizing RF exposure risks. Additional RF exposure information can be found on the FCC website at http://www.fcc.gov/oet/rfsafety/

3.3 Anti-Static Handling Procedures

The Open-Q 670 Hardware Development Kit has exposed electronics and chipsets. Proper anti-static precautions should be employed when handling the kit, including but not limited to:

- Using a grounded anti-static mat
- Using a grounded wrist or foot strap

3.4 Kit Contents

The Open-Q 670 Hardware Development Kit includes the following:

- A processor board with the Snapdragon™ 670 (SDA670) processor main CPU board
- Mini-ITX form-factor carrier board for I/O and connecting with external peripherals
- 12V power adapter
- USB type-C cable and charger
- 5.65” (1440x2160) Display card
- Lithium ion battery 4.4V/3000mAh

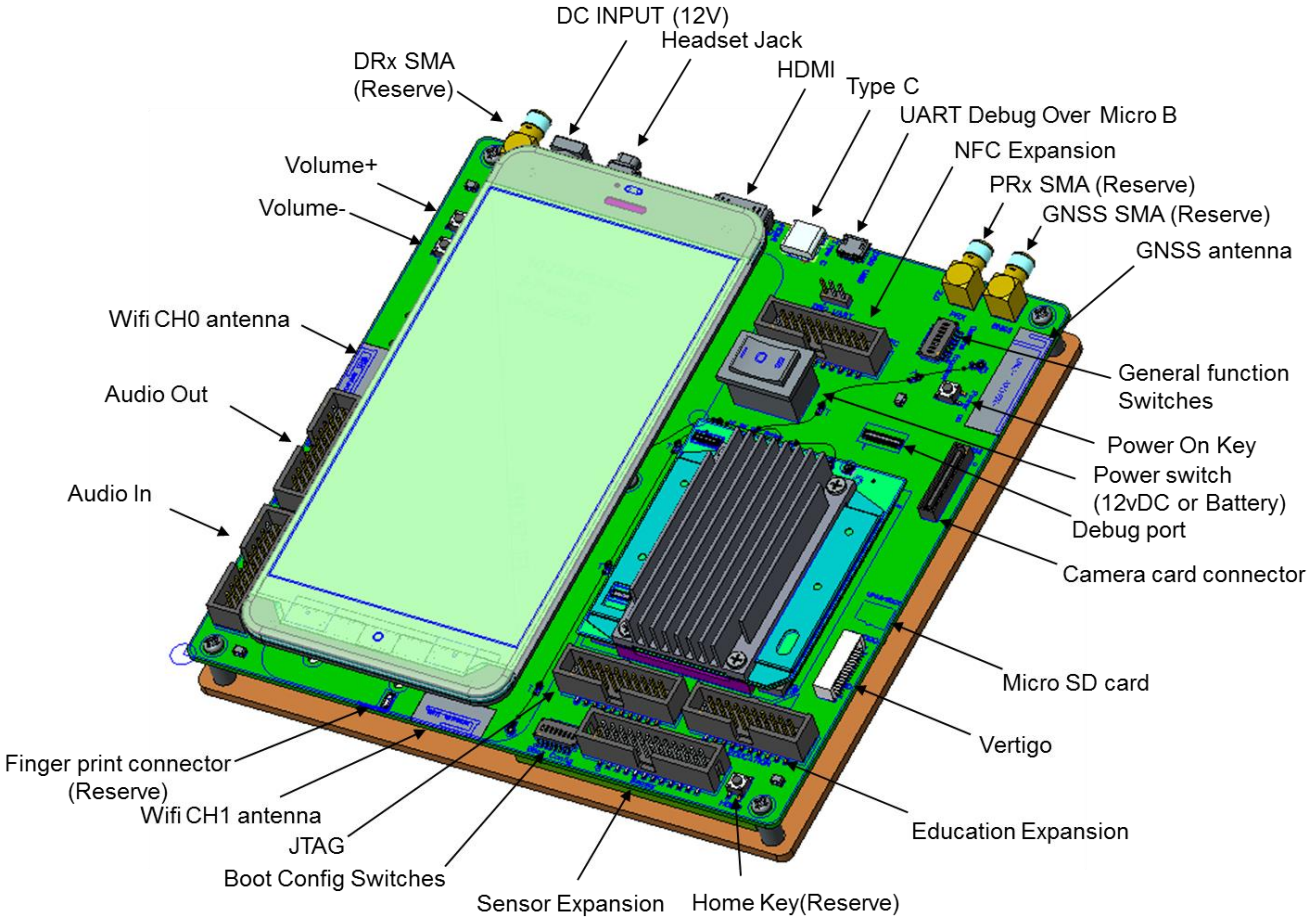

Figure 3-1 HDK670 Platform Top

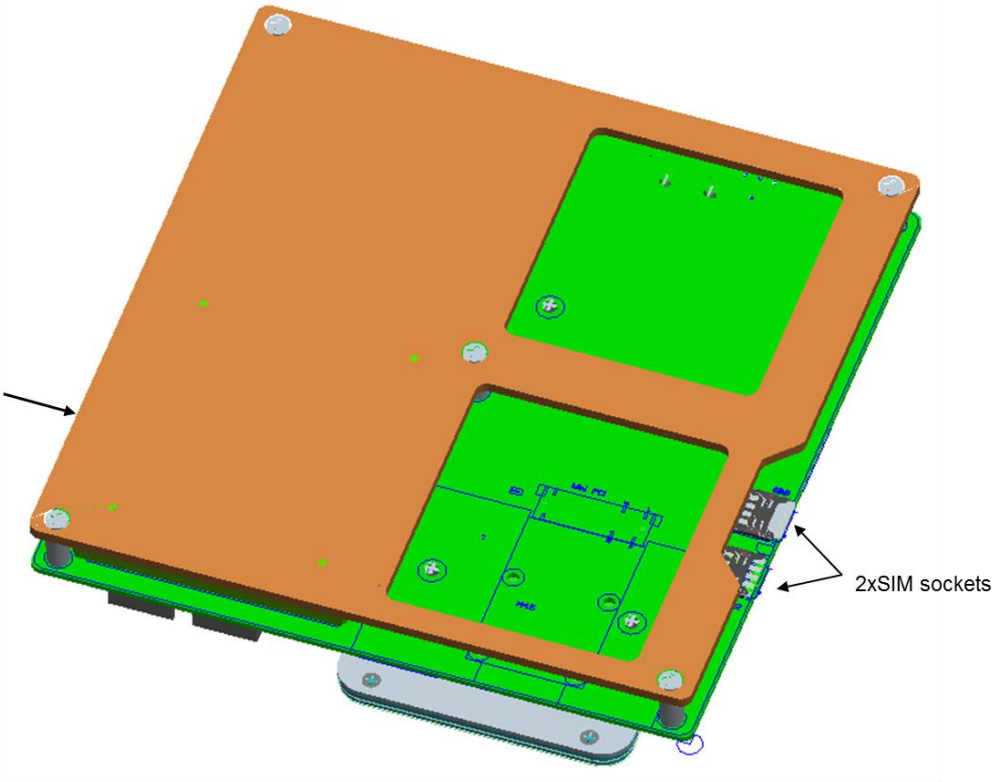

Figure 3-2 Assembled Open-Q 670 Hardware Development Kit bottom

The development kit comes with Android software pre-programmed on the CPU board or processor board. Please contact Intrinsyc for availability of camera modules, sensor boards, and other accessories: sales@intrinsyc.com

3.5 Hardware Identification Label

Labels are present on the CPU board. The following information is conveyed on these two boards:

Processor board:

- Serial Number
- WIFI MAC address

Refer to http://support.intrinsyc.com/account/serialnumber for more details about locating the serial number, as this will be needed to register the development kit. To register a development kit, please visit: http://support.intrinsyc.com/account/register

Note: Please retain the and carrier board serial number for warranty purposes.

3.6 System Block Diagram

The following diagram explains the interconnectivity and peripherals on the development kit.

The following diagram explains the interconnectivity and peripherals on the development kit.

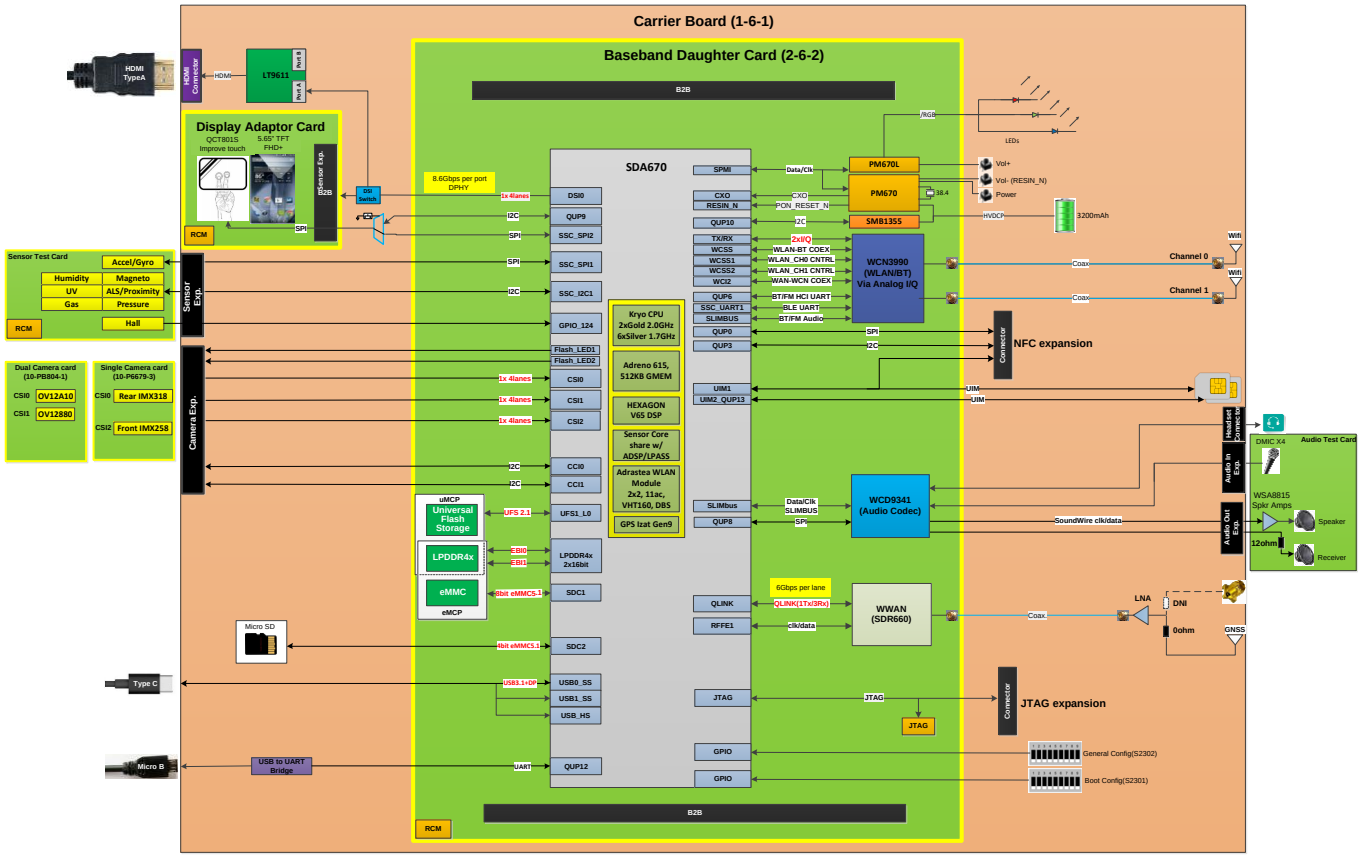

Figure 3-3 Open-Q 670 HDK Processor board + Carrier Board Block Diagram

3.7 Open-Q 670 HDK Processor Board

The Processor board provides the basic common set of features with minimal integration efforts for end users. It contains the following:

- Snapdragon 670 (SDA670) main application processor
- Memory (eMCP/uMCP compatible design)
- eMCP: 64GB eMMC 5.1 + LPDDR4x up to 1866MHz 6GB
- PMIC: PM670 + PM670L – PMIC for Peripheral LDOs, Boost Regulators
- SMB1355 Parallel charger
- WCN3990 Atheros Wi-Fi + BT +FM combo chip over SLIMbus, Analog IQ, UART, PCM
- WCD9341 Audio Code
- SDR660 GNSS support

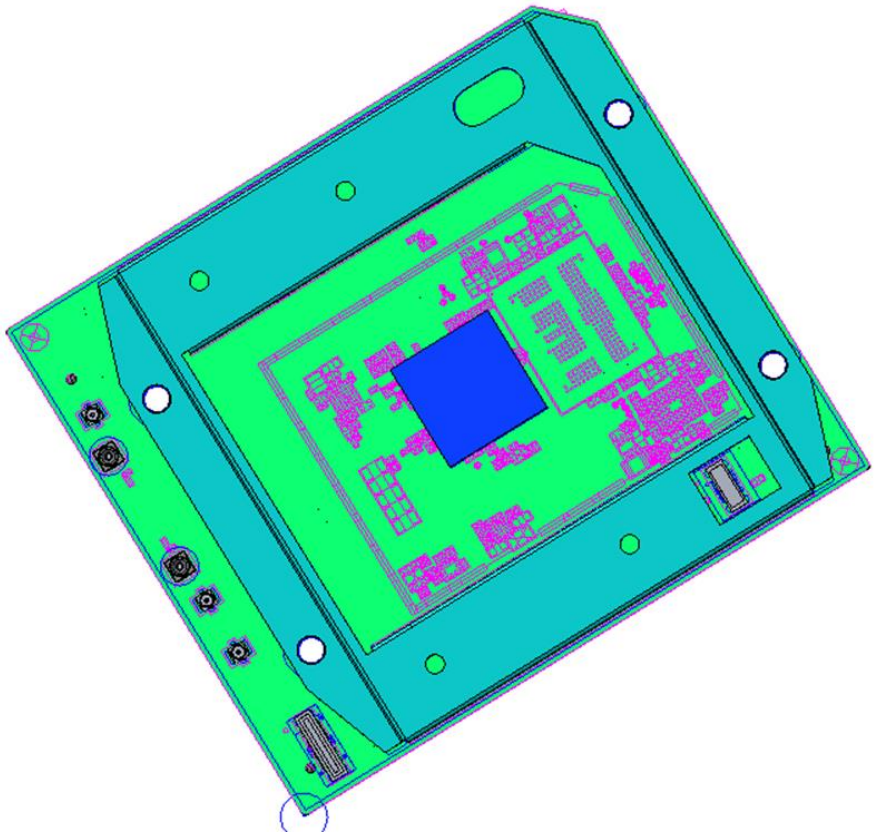

Figure 3-4 Open-Q 670 HDK PROCESSOR BOARD

3.7.1 Processor Board Mechanical Properties

Table 3.7-1 Open-Q 670 HDK Processor Board Mechanical Properties

Area	42 cm^2(60 mm x 70 mm)
Interface	2 x 240-pin high speed board to board connectors.
Thermal	A top side heat sink and a bottom side heat conductive metal plate are installed by default.

3.7.2 Processor Board Block Diagram

The Open-Q 670 HDK Processor board measuring 60mm x 70mm is where all the processing occurs. It is connected to the carrier via two 240-pin high speed board-to-board connector. The purpose of the connectors is to bring out essential signals such that other peripherals can interface with the platform.

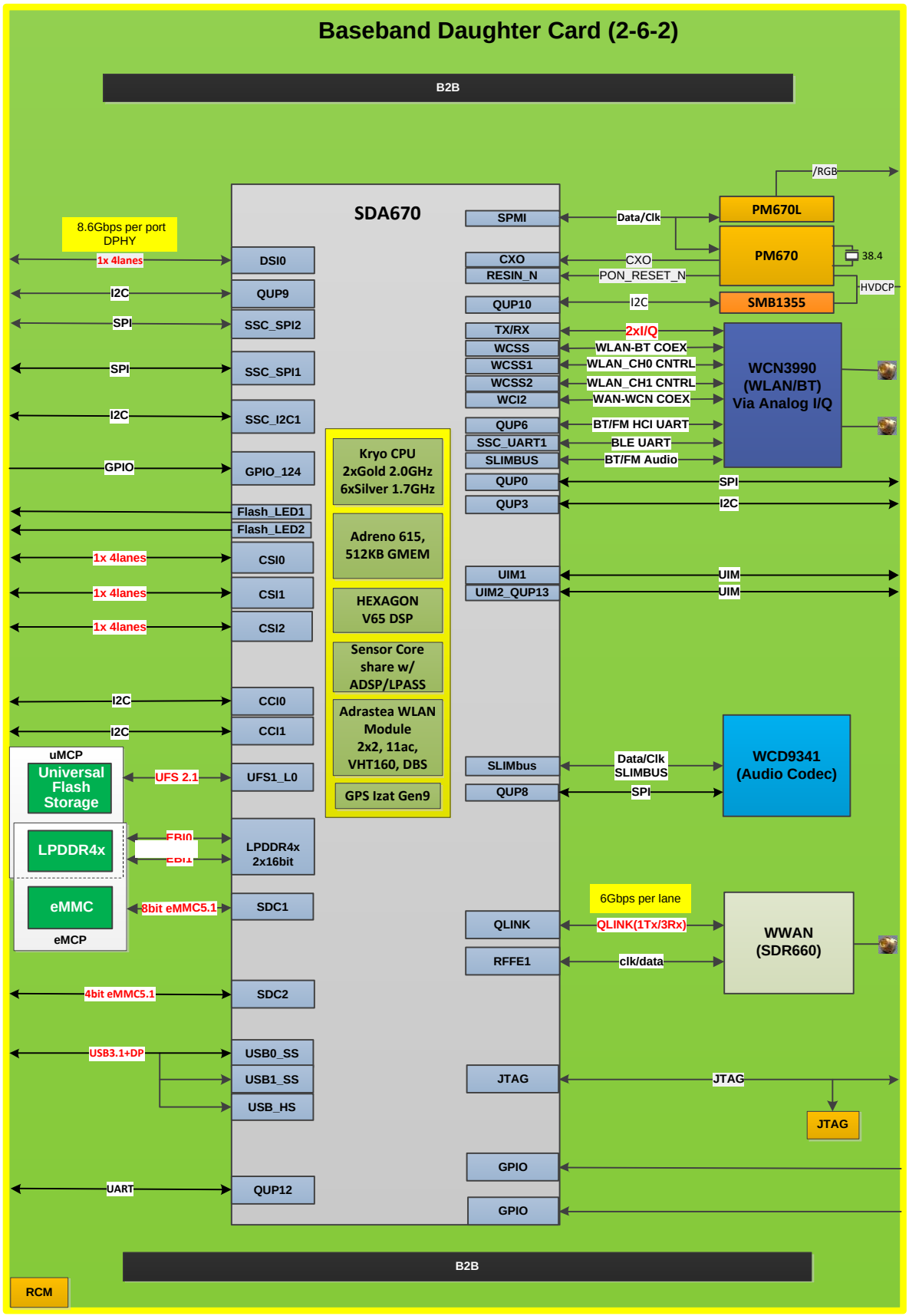

Figure 3-5 Open-Q 670 Processor Board Block Diagram

3.7.3 Hardware Specification

Table 3.7-2 Open-Q 670 HDK Processor Board Hardware Features

Subsystem / Connectors	Feature Set	Description	Specification
Chipset	SDA670	Qualcomm® Snapdragon™ 670 Processor	A customized 64-bit ARM v-8 compliant applications processor (Qualcomm® Kryo™ CPU 360) • Kryo Gold: dual high-performance cores 2.016 GHz • Kryo Silver: hexa low-power cores 1.708 GHz Adreno GPU 615 up to 430 MHz Low-power sensor over Hexagon DSP v65 (shared with low-power audio) 16/16/512 KB (with LPI)
	PMIC (PM670, PM670L)	Qualcomm® PMIC, Companion PMIC for SDA670 processor	PM670 – part of the dual PMIC solution that integrates wireless product's power management, general housekeeping, user interface, and IC-level interface support functions. PM670L – supplements the maser core PMIC(PM670) to integrate all wireless handset power management, general housekeeping, audio codec, and user interace support functions into an integrated two-IC solution, PM670L supports the LCD display module.
Memory	LPDDR4x	6GB LPDDR4X	LPDDR4x up to 1866MHz
	eMMC	64GB eMMC5.1	eMMC 5.1
	UFS	128GB UFS2.1	UFS 2.1
Connectivity	Wi-Fi 2.4 GHz/ 5GHz via WCN3990 – Analog IQ, WSI 2.0,	Wi-Fi Atheros WCN3990Wi-Fi + BT +FM Combo Chip	802.11a/b/g/n/ac 2.4/5.0 GHz via WCN3990 over analog IQ, WSI 2.0,
	BT 2.4 GHz via WCN3990 – UART / SLIMbus	Wi-Fi Atheros WCN3990 Wi-Fi + BT +FM Combo Chip	Support BT 5.0 + HS and backward compatible with BT 1.x, 2.x + EDR

Subsystem / Connectors	Feature Set	Description	Specification
	GNSS via SDR670 –Qlink Qualcomm Proprietary Protocol	GNSS Frontend	GPS/ GLONASS/ COMPASS/Galileo
RF	2xWLAN / BT	Connect to antenna on carrier board via coax cable	2.4/ 5 GHz
	1x GNSS	Connect to antenna on carrier board via coax cable	GPS/ GLONASS/ COMPASS /Galileo
Audio	1 x Headset Output	Headset/ headphone output	Analog differential output
	2 x Loud-speaker	2 x loud-speaker output	Digital output
	1 x Earpiece output	Earpiece output	Analog differential output
	3 x analog MICs	Analog MIC input	Analog differential input
	3 x digital MICs	Digital MIC input	Digital input
Camera	3 x MIPI CSI	1x 120pin Camera Connector for CSI0, CSI1, and CSI2	MIPI Allie Specification v1.2
Display	1 x MIPI DSI + Touch 100-pin display Connector	100- pin display connector	MIPI Allie Specification v1.2. MIPI D-PHY Specification v0.65, v0.81, v0.90, v1.01 ,v1.2
USB	1 x Type-C USB 3.1	Type-C USB 3.1	USB3.1
Connectors	2 x 240pin BB Card connector	Connector for BB Card	2 x 240 pin B2B connector

3.8 Open-Q 670 HDK Carrier Board

The Open-Q 670 HDK Carrier board is a Mini-ITX form factor board with various connectors used for connecting different peripherals. The following are the mechanical properties of the carrier board:

Table 3.8-1 Open-Q 670 HDK Carrier Board Mechanical Properties

Dimensions	289 cm^2 (170mm x 170mm)
Form Factor	Mini-ITX
Major Interfaces	Carrier board: 2x240 pin board to board connector Display: 100 pin board to board connector
Thermal	A thermal pad is placed between the processor board and the carrier board

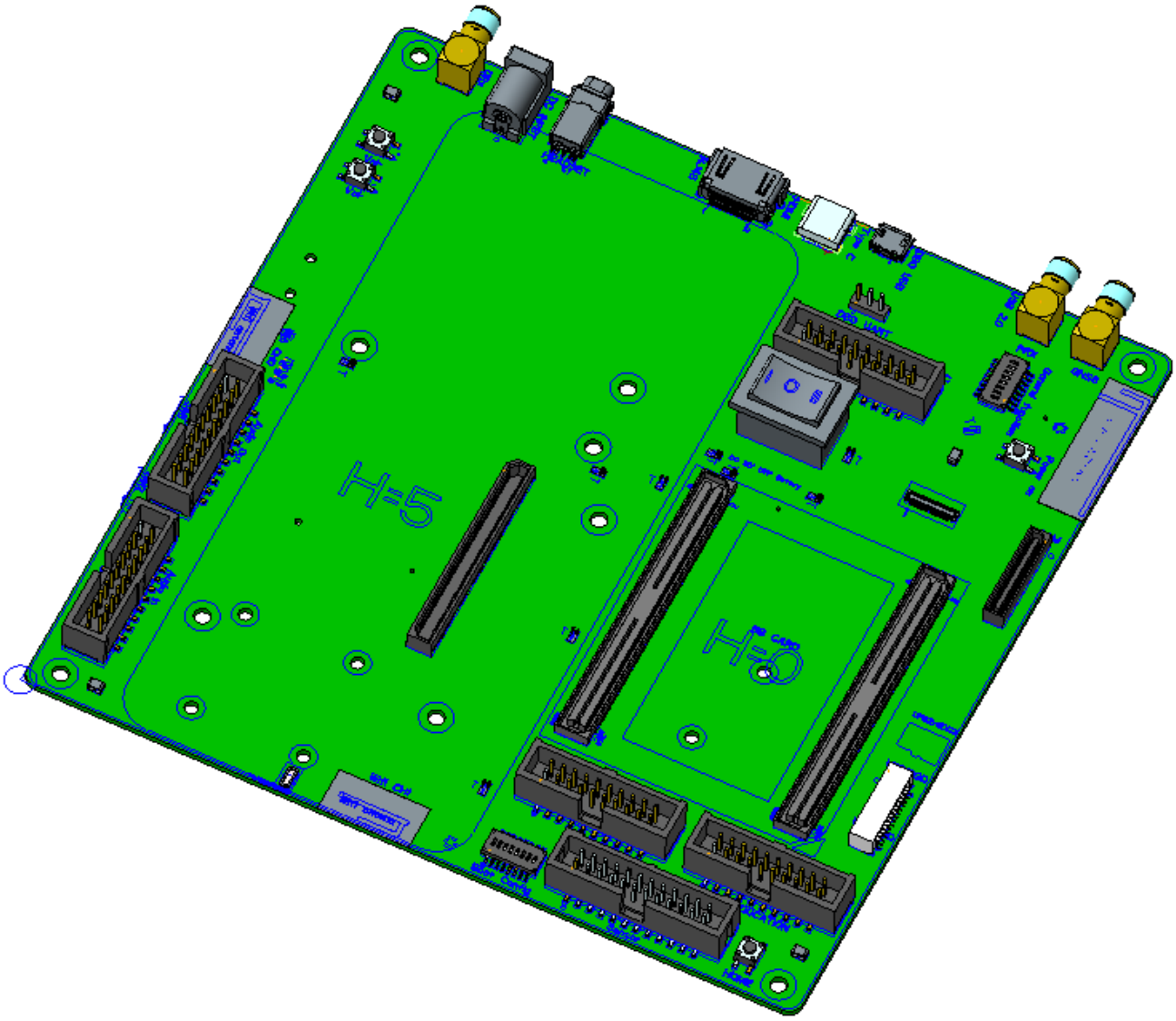

Figure 3-6 Open-Q 670 HDK Carrier Board

3.8.1 Dip switch Configuration Options

There is a DIP switch S2301 on the south top side of the Open-Q 670 HDK carrier board. The 8-bit switch allows the user to control the system configuration and boot options. Table 3.8-1 below outlines the pin outs and connections of this DIP switch.

Table 3.8-2 Dip Switch S2301 HW / SW configuration

Function	DIP Switch	Description	Notes
FORCED_USB_BOOT	S2301-1	Toggles between FORCE USB boot and EDL mode. Enables FOCE USB (GPIO 57) when DIP switch turned on	Default out of the box configuration is OFF
WATCHDOG _DISABLE	S2301-2	Enables WATCHDOG_DISABLE when DIP switch turned on. Controlled by SDA-GPIO 101	Default out of the box configuration is OFF
BOOT_CONFIG[1]	S2301-3	Enables SDA boot configuration 1 when DIP switch turned on. Controlled by SDA-GPIO 99	Default out of the box configuration is OFF
BOOT_CONFIG[2]	S2301-4	Enables SDA boot configuration 2 when DIP switch turned on. Controlled by SDA-GPIO100	Default out of the box configuration is OFF
BOOT_CONFIG[3]	S2301-5	Enables SDA boot configuration 3 when DIP switch turned on. Controlled by SDA GPIO133	Default out of the box configuration is OFF
External 5V boost manual control (Reserve)	S2301-6	Manually enable external 5V boost output. Default controlled by software automatically	Default out of the box configuration is OFF This DIP is default disabled and for internal use only.
DSI0_SW_SEL(Reserve)	S2301-7	Select DSI0 data path between display card and HDMI Default route DSI0 to display card	Default out of the box configuration is OFF This DIP is default disabled. DSI0 data path is default simultaneously controlled by S2301-8 for easy use. To separately control DSI0 path with this DIP needs HW change (DNI R3404, SMT R3403).
DSI1_SW_SEL	S2301-8	Select DSI1 data path between display and HDMI Default route DSI1 to display card	Default out of the box configuration is OFF DSI1 will be routed to HDMI by turning on DIP. This DIP controls both DSI0 and DSI1 by default.

There is another DIP switch S2302 on the north top side of the carrier board. The 8-bit switch allows the user to control the system configuration and boot options.

Table 3.8-3 Dip Switch S2302 HW / SW configuration

Function	DIP Switch	Description	Notes
CHARGE_DISABLE	S2302-1	Disable charge when DIP switch turned on	Default out of the box configuration is OFF which enables system charge from USB **Note:** make sure turn on this switch when DC-12V input and USB are both present
N/C	S2302-2	NA	Not used in HDK670
N/C	S2302-3	NA	Not used in HDK670
MSM_PS_HOLD	S2302-4	Enables the JTAG_PS_HOLD mode when DIP switch turned on	Default out of the box configuration is OFF
N/C	S2302-5	NA	Not used in HDK670
QUP0_SPI_SEL	S2302-6	Select QUP0 path between NFC(J2401) and Education(J2801)/ETH	Default out of the box configuration is OFF **Note:** QUP0 is default routed to NFC
QUP15_SPI_SEL	S2302-7	Select QUP15 path between display card (J1301) and onboard fingerprint(J3102)	Default out of the box configuration is OFF **Note:** QUP15 is default routed to onboard fingerprint
QUP_TP_CONFIG	S2302-8	Config the signals connected to QUP_TP	Default out of the box configuration is OFF **Note:** SSC SPI2 is routed to QUP_TP by default

Warning! : Before making any changes to the dip switch, make sure to note down the previous configuration. The default switch settings are above.

3.8.2 Carrier Board Expansion Connectors

The following table lists the connectors, expansions and their usages on the carrier board:

Table 3.8-4 Carrier Board Expansion Options and Usage

Domain	Description	Specification	Usage
Power	AC / Barrel charger	12 V DC Power Supply 5 A	Power Supply
	Battery connector	8 pin header	For providing power from 4.4V/2850mAh battery
Debug Serial via USB	Debug Serial UART console over USB for development	USB Micro B connector	Development Serial Connector for debug output via USB
JTAG	OS / Firmware /QFROM Programming / Debugging JTAG	Standard 20-pin connector, ARM and OpenDSP – Lauterbach	QFROM / eMMC / Platform EEPROM programming ARM / Open DSP debugging
Buttons	Power	SMD Button	Power Button for Suspend / Resume and Power off
	Volume +	SMD Button	Volume +Key
	Volume –	SMD Button	Volume – Key
	Home(Reserve)	SMD Button	Reserved button for Home or general purpose
NFC Board Header	20 pin NFC expansion connectors	Standard 20-pin connector, support dedicated NFC debug card	Reserved connector for internal use
Micro SD Card	Micro SD card	4bit Micro SD card support	External Storage
Audio Jack	Audio Jack Supported by WCD9341	Nomal Open, support US Standard CTIA headset by default	Audio headset support
3-Digital Microphone via audio input expansion header	Audio expansion Supported by WCD9341	Digital Audio header	For Digital audio input for Digital MIC, I2S codec, Slim bus interface.
3-Analog Microphone via audio input expansion header	Audio expansion Supported by WCD9341	Analog Audio header	For Analog audio input for Analog MIC (differential signal)
2-Loud Speaker via audio output expansion header	Audio expansion Supported by WCD9341	Analog Audio header	For loud speaker output after signal has been processed
Earpiece via audio output expansion header	Audio expansion Supported by WCD9341	Analog Audio header	For earpiece output after signal has been processed
USB 3.1	USB 3.1	Type-C header	Transfer data to and from CPU
WLAN Antenna	2X PCB Antenna	2.4 – 5 GHz	Antenna to BB card

Domain	Description	Specification	Usage
GNSS Antenna	PCB Antenna	GPS : 1574.42 MHz – 1576.42 MHz GLONASS : 1587 MHz – 1606 MHz COMPASS: 1559.05 to 1563.14MHz Galileo: 4.092MHz BW(centered on 1575.42MHz)	Antenna to BB card
LED	3xLED	Red : PMIC Driven Green: PMIC Driven Blue: PMIC Driven	Red : General purpose Green : General purpose Blue : General purpose
LCD Display and Touch connector	100 pin for LCD signals from B2B boards for display	4-lane MIPI DSI0 , DSI1 I2C/SPI/GPIO Backlight MIPI Allie Specification v1.2 MIPI D-PHY Specification v0.65,v0.81, v0.90, v1.01, V1.2 MIPI C-PHY Specification v1.0	Only 1 lane DSI is supported on HDK670
Sensor header	24 pin sensor header	24 pin sensor header	Header to connect sensor board.
SIM Card	WWAN SIM card connector (Reserve)	2x 4bit Micro SIM card support	For WWAN mini PCI express cards (for internal use only – not supported)
CSI Camera connectors	1 x 120pin connector with MCLK, GPIOS, CCI 1 x 120pin connector with MCLK, GPIOS, CCI	Supports CSI0, CSI1 and CSI2 via one 120pin connector ▪ 3 x MIPI-CSI each 4 lane ▪ External flash driver control ▪ Support for 3D camera configuration ▪ Separate MCLK / CCI control MIPI Allie Specification v1.2 for Camera Serial Interface	▪ Single Rear, Front camera ▪ Dual Camera ▪ Iris Camera

The following sections provide in depth information on each expansion headers and connectors on the carrier board. The information listed below is of particular use for those who want to interface other external hardware devices with the Open-Q 670 HDK. **Before connecting anything to the development kit, please ensure the device meets the specific hardware requirements of the processor.**

3.8.2.1 Power Options

The Open-Q 670 Hardware Development Kit power source connects to the 12V DC power supply jack J0701. Starting from the power jack, the 12V power supply branches off into different voltage rails via step down converters on the carrier board and PMIC on the Processor board. The Processor board is powered by 3.9V via a Silergy step down converter U0703 on the carrier board.

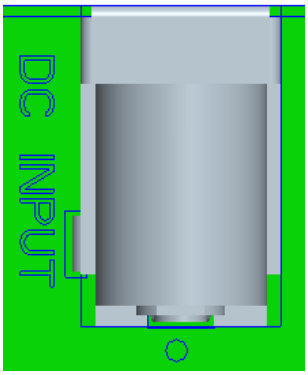

Figure 3-7 J0701 12V DC Power Jack

The Processor board has 2 PMIC modules: PM670 and PM670L Functionalities of the two modules are outlined below:

- Source various regulated power rails
- Source system clock
- Support for battery charging

The charging port in PM670 is configurable on the platform. The carrier board can either use a 3.9V constant power input or battery to supply the processor card. A DIP switch is used to enable/disable charge function. Make sure to turn off battery charging when 12V DC in is used and USB charger is inserted.

3.8.2.2 Debug Serial UART header J2103

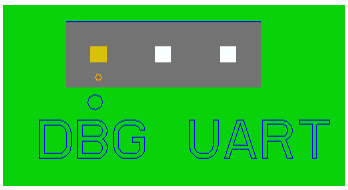

Figure 3-8 J2103 3.3V TTL Debug UART

The header consists of TX, RX and GND pins. It is a 3.3V TTL UART header. To get the serial terminal working with a PC, the following cable (or similar) is needed

http://www.digikey.ca/product-detail/en/TTL-232R-RPI/768-1204-ND/4382044

Table 3.8-5 Debug UART Header J2103 Pin-out

Description	Signal	pin	FTDI RPI cable connection
SDA UART RX (GPIO52)	QUP12_UART_RX	J2103[1]	Orange
SDA UART TX (GPIO51)	QUP12_UART_TX	J2103[2]	Yellow
GND	GND	J2103[3]	Black

3.8.2.3 Debug Serial UART over USB J2102

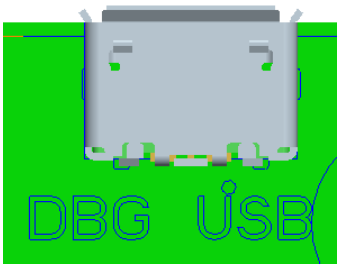

Figure 3-9 J2102 Debug UART over USB

The UART connection used on the HDK is a USB micro B connector (J2102). This debug UART is available over USB via the FTDI FT232RQ chip on the carrier board. To get the serial terminal working with a PC, user needs to ensure that the appropriate FTDI drivers are installed.

3.8.2.4 JTAG header J2101

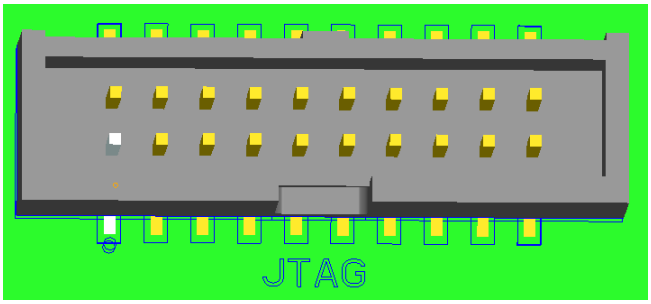

Figure 3-10 J2101 JTAG header

This connector provides a JTAG interface to the main processor by which users can connect a JTAG (Lauterbach / USB Wiggler) 20 pin ARM JTAG.

NOTE: The development kit does not include software support for JTAG

Table 3.8-6 JTAG Header J2101 Pin out

Description	Signal	Pin NO	Description	Signal	Pin NO
GND	GND	J2101[2]	JTAG Power detect	JTAG_PWR	J2101[1]
GND	GND	J2101[4]	Target RESET_N signal	TRST_N	J2101[3]
GND	GND	J2101[6]	TDI Signal (Target DATA IN)	TDI	J2101[5]
GND	GND	J2101[8]	TMS Signal	TMS	J2101[7]
GND	GND	J2101[10]	TCK Signal	TCK	J2101[9]
GND	GND	J2101[12]	JTAG_RTCK signal	JTAG_RTCK	J2101[11]
GND	GND	J2101[14]	TDO Signal (Target Data Out)	TDO	J2101[13]
GND via 4.7KΩ pull down	GND	J2101[16]	Source RESET_N signal	SRST_N	J2101[15]
GND	GND	J2101[18]	NC	NC	J2101[17]
JTAG detect N signal	DET_N	J2101[20]	GND via 4.7KΩ pull down	GND	J2101[19]

3.8.2.5 Sensor IO Expansion Header J2501

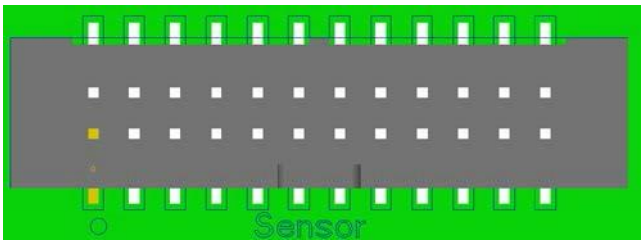

Figure 3-11 J2501 SENSOR EXPANSION HEADER

The sensor expansion header J2501 allows for a 24-pin connection to an optional sensor board. If user application does not require a sensor, then this header can be used for other applications that require I2C or GPIO input and output connections.

Following is the pin breakout for sensor expansion header J2501

Table 3.8-7 Sensor Expansion Header J2501 Pin out

Description	Signal	Pin NO	Description	Signal	Pin NO
SSC I2C1 serial data	SSC_I2C1_SDA	J2501[1]	Accelerometer interrupt input to processor via GPIO117	ACCEL_INT	J2501[2]
SSC I2C1 serial clock	SSC_I2C1_SCL	J2501[3]	Cap interrupt input to processor via GPIO123	PRESS_INT_N	J2501[4]
Sensor reset signal from processor to sensor via GPIO44	MEMS_RESET_N	J2501[5]	Gyroscope interrupt input to processor via GPIO118	GYRO_INT	J2501[6]
Sensor IO PWR 1.8 V VREG_LVS2A_1P8 power supply regulator (Digital)	SENS_IO_PWR	J2501[7]	Sensor Analog power supply from VREG_L19A 2.85V or 3.3V	SENS_ANA_PWR	J2501[8]
GND	GND	J2501[9]	GND	GND	J2501[10]
HRM interrupt/ configurable GPIO122	HRM_INT	J2501[11]	Touch screen interrupt input from processor via GPIO125	TS_INT_N	J2501[12]
SSC SPI-1 chip select 2	SSC_SPI1_CS1_N	J2501[13]	ALS/P sensor interrupt input to processor via GPIO120	ALSP_INT_N	J2501[14]
MISC GPIO for sensor via GPIO43	SDA_GPIO	J2501[15]	Digital Compass interrupt input to processor via GPIO119	MAG_DRDY_INT	J2501[16]
NC	NC	J2501[17]	Hall sensor interrupt input to processor via GPIO124	HALL_INT_N	J2501[18]
SSC SPI-1 chip select 1	SSC_SPI1_CS0_N	J2501[19]	SSC SPI-1 data master out/ slave in	SSC_SPI_1_MOSI	J2501[20]
SSC SPI-1 clock	SSC_SPI1_CLK	J2501[21]	SSC SPI-1 data master in/ slave out	SSC_SPI_1_MISO	J2501[22]
NC	NC	J2501[23]	SSC SPI-1 chip select 3	SSC_SPI1_CS2_N	J2501[24]

In summary, if sensor application is not needed, this expansion header can provide SSC SPI1 and I2C. Please refer to the schematic and consider the power before connecting anything to this header.

3.8.2.6 NFC Expansion Header J2401

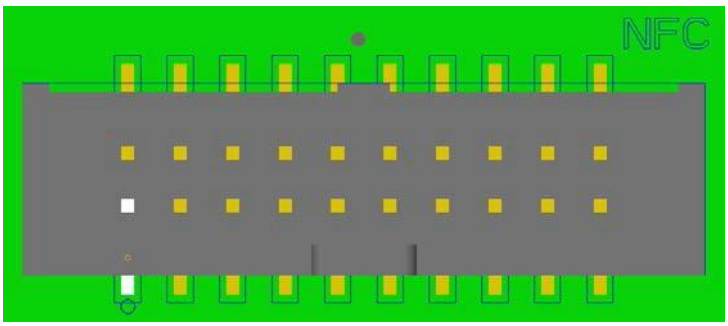

Figure 3-12 J2401 NFC EXPANSION HEADER

The NFC expansion header provides a 20 pin connector for attaching an optional NFC board. This header also allows user to connect to the free GPIOs and I2C lines when NFC is not used; therefore, enabling other use cases. Please refer to Table below for detailed information regarding the signals that are being brought out by this connector.

Table 3.8-8 NFC Expansion Header J2401 pin out

Description	Signal	Pin NO	Description	Signal	Pin NO
QUP0 via SDA GPIO2	NFC_SPI_CLK	J2401[1]	QUP0 via SDA GPIO0	NFC_SPI_MISO	J2401[2]
NFC power request via GPIO116	NFC_ESE_PWR_REQ	J2401[3]	SIM present GPIO via SDA GPIO112	UMI1_DET_N	J2401[4]
SIM Card DATA line (UIM1) via SDA GPIO109	UIM1_DATA	J2401[5]	3.9V BB CARD power supply pin	VPH_PWR	J2401[6]
SIM Card Reset line (UIM1) via SDA GPIO111	UIM1_RESET	J2401[7]	NFC interrupt IRQ pin via SDA GPIO44	NFC_IRQ	J2401[8]
SIM CLK line (SIM1) via SDA GPIO110	UIM1_CLK	J2401[9]	NFC Disable signal via SDA GPIO12	NFC_ENABLE	J2401[10]
1.8V Voltage regulator supply max 150mA via PM670	VREG_L9A_1P8	J2401[11]	QUP3 I2C SDA line	NFC_I2C3_SDA	J2401[12]
1.8V Voltage regulator supply via PM670	VREG_S4A_1P8	J2401[13]	QUP3 I2C CLK line	NFC_I2C3_SCL	J2401[14]
GND	GND	J2401[15]	NFC clock request signal via PM670 GPIO3	NFC_LNBBCLK3_EN	J2401[16]
PM670 free running clock via buffer	LN_BB_CLK3_NFC	J2401[17]	NFC download request via SDA GPIO43	NFC_DWL_REQ	J2401[18]
QUP0 via SDA GPIO3	NFC_SPI_CS_N	J2401[19]	QUP0 via SDA GPIO1	NFC_SPI_MOSI	J2401[20]

In general, if there is no need for NFC application, this expansion header can provide two GPIOs, I2C, free running clocks, and enable voltage/ power source to external peripherals.

3.8.2.7 Headset Jack J1501

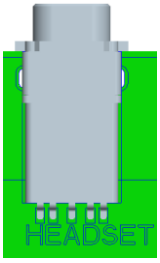

Figure 3-13 HEADPHONE JACK

The headset jack (J1501) is a standard 3.5mm, Normal Open Style jack. The hardware supports US Standard CTIA headset by default.

3.8.2.8 Audio Inputs Expansion Header J1601

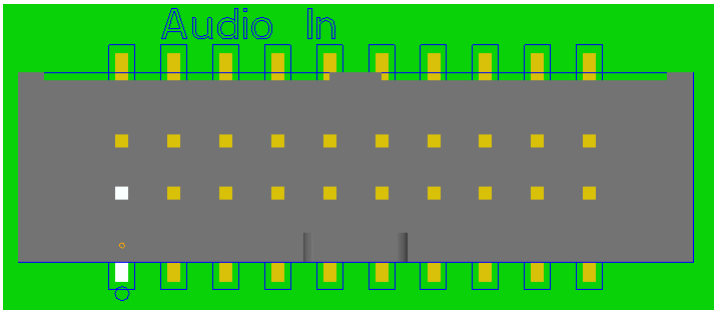

Figure 3-14 J1601 Audio Inputs Expansion Header

This header expansion provides the following audio inputs:

- 3 digital mics
- 3 analog mics
- Voltage rails to support analog and digital mics

The table below outlines the pin out information of the audio inputs expansion header J1601:

Table 3.8-9 Audio Inputs Expansion Header J1601 Pin out

Description	Signal	Pin NO	Description	Signal	Pin NO
Analog MIC1 positive differential input	CDC_IN1_P	J1601[1]	Analog MIC1 negative differential input	CDC_IN1_N	J1601[2]
Analog MIC2 positive differential input	CDC_IN3_P	J1601[3]	Analog MIC2negative differential input	CDC_IN3_N	J1601[4]
MIC bias output voltage 1	MIC_BIAS1	J1601[5]	MIC bias output voltage 3	MIC_BIAS3	J1601[6]
Analog MIC3 positive differential input	CDC_IN4_P	J1601[7]	Analog MIC3 negative differential input	CDC_IN4_N	J1601[8]
MIC bias output voltage 4	MIC_BIAS4	J1601[9]	3.3V power supply max 500mA	MB_VREG_3P3	J1601[10]
GND	GND	J1601[11]	GND	GND	J1601[12]
Clock for digital MIC3	CDC_DMIC_CLK1	J1601[13]	Clock for digital MIC1	CDC_DMIC_CLK2	J1601[14]
Digital MIC3data line	CDC_DMIC_DATA1	J1601[15]	Digital MIC1data line	CDC_DMIC_DATA2	J1601[16]
1.8V power supply max 300mA	VREG_S4A_1P8	J1601[17]	Clock for digital MIC2	CDC_DMIC_CLK3	J1601[18]
GND	GND	J1601[19]	Digital MIC2data line	CDC_DMIC_DATA3	J1601[20]

3.8.2.9 Audio Outputs Expansion Header J1602

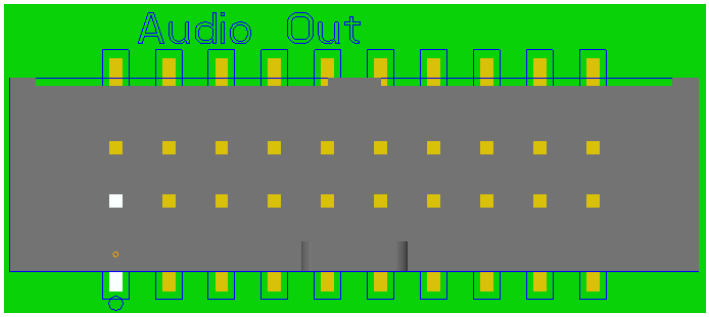

Figure 3-15 J1602 Audio Outputs Expansion Header

This header expansion provides the following audio outputs:

- 2 differential analog audio line out
- 2 single ended analog audio line out
- 1 differential analog earpiece amplifier output (no external amp needed)
- 2 speaker amplifier enable control
- Voltage rails to support analog and digital mics

The table below outlines the pin out information of the audio outputs expansion header J1602:

Table 3.8-10 Audio Inputs Expansion Header J1601 Pin out

Description	Signal	Pin NO	Description	Signal	Pin NO
Analog audio line out 1, positive differential output	LINE_OUT1_P	J1602[1]	Analog audio line out 1, negative differential output	LINE_OUT1_N	J1602[2]
Analog audio line out 2, positive differential output	LINE_OUT2_P	J1602[3]	Analog audio line out 2, negative differential output	LINE_OUT2_N	J1602[4]
Audio line single end outputs GND reference(connect to ground)	LINE_REF	J1602[5]	3.3V output power supply	MB_VREG_3P3	J1602[6]
Analog audio line out 1, single ended output	LINE_OUT1_P	J1602[7]	Analog audio line out 2, single ended output	LINE_OUT2_P	J1602[8]
Analog earpiece amplifier out, positive differential output	CDC_EAR_P	J1602[9]	Analog earpiece amplifier out, negative differential output	CDC_EAR_M	J1602[10]
GND	GND	J1602[11]	3.8V output power supply	VPH_PWR	J1602[12]
Digital sound wire data for WSA8810/ WSA8815 smart speaker amplifier	CDC_SWR_CLK	J1602[13]	Digital sound wire data for WSA8810/ WSA8815 smart speaker amplifier	CDC_SWR_DATA	J1602[14]
Speaker amplifier enable 1	WSA_EN	J1602[15]	Speaker amplifier enable 2	SPKR_AMP_EN2	J1602[16]
1.8V output power supply	VREG_S4A_1P8	J1602[17]	12V output power supply	DC_IN_12V	J1602[18]
5.0V output power supply	MB_VREG_5P0	J1602[19]	GND	GND	J1602[20]

3.8.2.10 USB3.1 Type-C Connector J1201

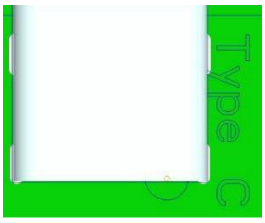

Figure 3-16 J1201 USB3.1 Type-C Connector

The on-board Type-C connector supports USB 3.1 Gen1, which also supports Type-C with DisplayPort V1.3.

3.8.2.11 On Board PCB WLAN Antenna

The HDK carrier board has two on-board PCB antennas that connects to the WCN3990 WiFi module on the processor board via coaxial cables that attaches to MH4L receptacles. These antennas connect to the processor board in the following configuration:

- WIFI CH0 on the carrier board connects to ANT0 on the WCN3990 WiFi module
- WIFI CH1 on the carrier board connects to ANT1 on the WCN3990 WiFi module

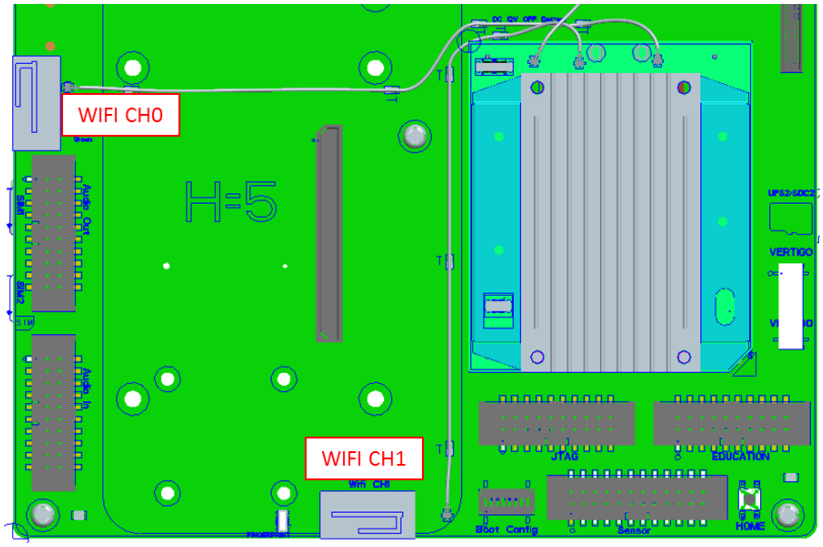

Figure 3-17 On Board PCB WLAN Antennas

3.8.2.12 On Board PCB GNSS Antenna

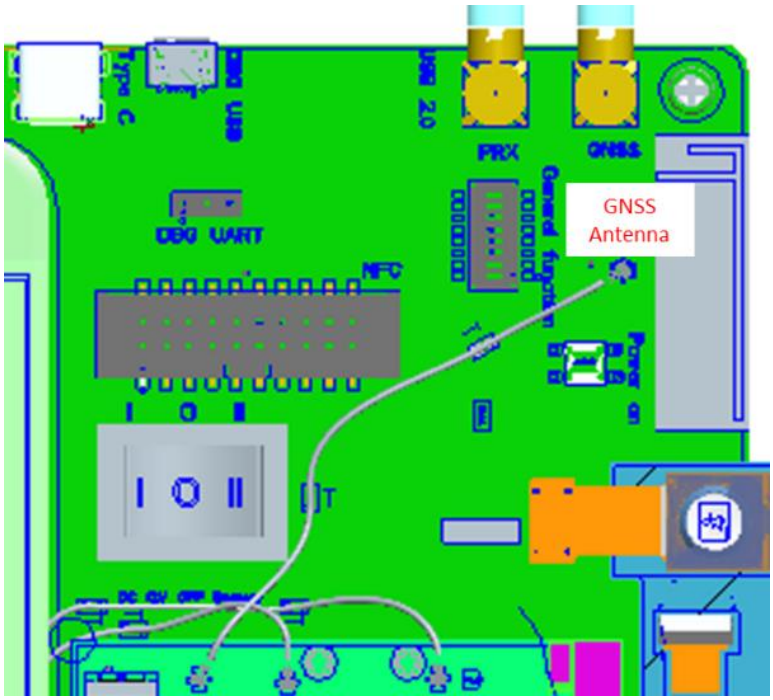

Figure 3-18 On board PCB GNSS Antennas

The HDK carrier board has one on-board PCB antenna on the bottom side that connects to the processor board via coaxial cable that attaches to MH4L receptacles. The on-board antenna is connected to the processor board by default, there are 0ohm jumpers for user to use an external GNSS antenna via the SMA connector. The option pads are between the antenna and the eLNA input.

Table 3.8-11 GNSS Antenna Option

Option	R3804	R3805
On-Board	DNI	Stuff
SMA connector	Stuff	DNI

3.8.2.13 GNSS SMA Connector J3802

The GNSS SMA connector is reserved for user to use an external antenna. Refer to Table 3.8-11, stuff R3804 and remove R3805 to make the path active.

Figure 3-19 GNSS SMA Connector

3.8.2.14 Camera connectors

The HDK development kit supports three 4-lane MIPI camera interfaces via a 120pin connector, it also supports one 2-lane MIPI camera interface via a 23pin connector on the processor card.

The following are some features of the camera connectors:

- 3 x 4 lane MIPI CSI signals, CSI0, CSI1 and CSI2
- Support for 3D camera configuration
  - Separate I2C control (CCI0, CCI1)
- Self-regulated camera modules can be powered with 3.3V power (MB_VREG_3P3)
- Uses Amphenol 11826-ACA connector for exposing MIPI, MCLK, CCI, GPIOs and Power rails.
- Please use Amphenol 11828-1CA mating connector to access these signals.

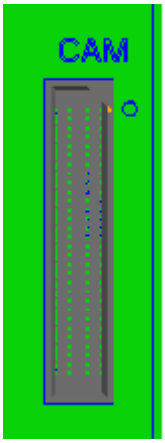

Figure 3-20 Camera Connector (J1701)

Table 3.8-12 MIPI CSI Camera Connector Pinouts (J1701)

Pin#	Signal	Description	Pin#	Signal	Description
A1	CAM_VREG_3P3	3.3V power supplier	B1	DGND	
A2	CAM_VREG_3P3	3.3V power supplier	B2	CCI_I2C_SDA0	SDA GPIO17
A3	CAM_VREG_3P3	3.3V power supplier	B3	CCI_I2C_SCL0	SDA GPIO18
A4	DGND		B4	DGND	
A5	CAM_S5A	2.04V power supplier	B5	CCI_I2C_SDA1	SDA GPIO19
A6	P1V8_CAM_IOVDD	1.8V power supplier	B6	CCI_I2C_SCL1	SDA GPIO20
A7	DGND		B7	DGND	
A8	FLASH_LED1	FLASHLED1	B8	CAM_S3A	1.35V power supplier
A9	FLASH_LED1	FLASHLED1	B9	CAM_S3A	1.35V power supplier
A10	DGND		B10	DGND	
A11	FLASH_LED2	FLASHLED2	B11	CAM_ELDO4_EN	PM670 GPIO9
A12	FLASH_LED2	FLASHLED2	B12	CAM_ELDO1_EN	PM670 GPIO12
A13	DGND		B13	DGND	
A14	FLASH_LED3	FLASHLED3	B14	NC	
A15	FLASH_LED3	FLASHLED3	B15	FLASH_R3LED_EN	PMI8998 GPIO3
A16	DGND		B16	DGND	
A17	MIPI_CSI2_LANE3_N	CSI2 data	B17	FLASH_FRONT_EN	SDA GPIO21
A18	MIPI_CSI2_LANE3_P	CSI2 data	B18	FL_STROBE_TRIG	SDA GPIO22
A19	DGND		B19	DGND	
A20	MIPI_CSI2_LANE2_N	CSI2 data	B20	P1V8_CAM_IOVDD	1.8V power supplier
A21	MIPI_CSI2_LANE2_P	CSI2 data	B21	P1V2_DVDD_CAM1_2	1.2V power supplier
A22	DGND		B22	DGND	

Pin#	Signal	Description	Pin#	Signal	Description
A23	MIPI_CSI2_LANE1_N	CSI2 data	B23	P2V85_AVDD_CAM1_2	2.85V power supplier
A24	MIPI_CSI2_LANE1_P	CSI2 data	B24	P2V85_AVDD_CAM1_2	2.85V power supplier
A25	DGND		B25	DGND	
A26	MIPI_CSI2_LANE0_N	CSI2 data	B26	P2V8_VCM_LASER_RF	2.8V power supplier
A27	MIPI_CSI2_LANE0_P	CSI2 data	B27	P2V8_VCM_LASER_RF	2.8V power supplier
A28	DGND		B28	DGND	
A29	MIPI_CSI2_CLK_N	CSI2 clock	B29	P1V2_DVDD_CAM1_2	1.2V power supplier
A30	MIPI_CSI2_CLK_P	CSI2 clock	B30	P1V2_DVDD_CAM1_2	1.2V power supplier

Pin#	Signal	Description	Pin#	Signal	Description
C1	CAM_MCLK0_BUF	SDA GPIO13	D1	DGND	
C2	CAM0_RSTN	SDA GPIO80	D2	MIPI_CSI0_LANE3_N	CSI0 data
C3	CAM_ELDO9_EN	SDA GPIO79	D3	MIPI_CSI0_LANE3_P	CSI0 data
C4	DGND		D4	DGND	
C5	CAM1_RSTN	SDA GPIO28	D5	MIPI_CSI0_LANE2_N	CSI0 data
C6	CAM_ELDO3_EN	SDA GPIO27	D6	MIPI_CSI0_LANE2_P	CSI0 data
C7	CAM_MCLK1_BUF	SDA GPIO14	D7	DGND	
C8	DGND		D8	MIPI_CSI0_LANE1_N	CSI0 data
C9	CAM2_RSTN	SDA GPIO9	D9	MIPI_CSI0_LANE1_P	CSI0 data
C10	CAM_MCLK2_BUF	SDA GPIO15	D10	DGND	
C11	CAM_ELDO2_EN	SDA GPIO8	D11	MIPI_CSI0_LANE0_N	CSI0 data
C12	DGND		D12	MIPI_CSI0_LANE0_P	CSI0 data
C13	CAM_MCLK3_BUF	SDA GPIO16	D13	DGND	
C14	CAM3_RSTN	SDA GPIO23	D14	MIPI_CSI0_CLK_N	CSI0 clock
C15	OIS_SYNC	SDA GPIO25	D15	MIPI_CSI0_CLK_P	CSI0 clock
C16	DGND		D16	DGND	
C17	LASER_IRQ	SDA GPIO26	D17	MIPI_CSI1_LANE3_N	CSI1 data
C18	LASER_CE	SDA GPIO100	D18	MIPI_CSI1_LANE3_P	CSI1 data
C19	DGND		D19	DGND	
C20	P2V8_CAMA3	NC	D20	MIPI_CSI1_LANE2_N	CSI1 data
C21	P2V8_VCM_LASER_RF	2.8V power supplier	D21	MIPI_CSI1_LANE2_P	CSI1 data
C22	DGND		D22	DGND	
C23	CAM_IRQ	SDA GPIO24	D23	MIPI_CSI1_LANE1_N	CSI1 data

Pin#	Signal	Description	Pin#	Signal	Description
C24	NC		D24	MIPI_CSI1_LANE1_P	CSI1 data
C25	DGND		D25	DGND	
C26	P2V85_CAM0_AVDD	2.85V power supplier	D26	MIPI_CSI1_LANE0_N	CSI1 data
C27	NC		D27	MIPI_CSI1_LANE0_P	CSI1 data
C28	DGND		D28	DGND	
C29	P1V05_DVDD_CAM0	1.05V power supplier	D29	MIPI_CSI1_CLK_N	CSI1 clock
C30	P1V05_DVDD_CAM0	1.05V power supplier	D30	MIPI_CSI1_CLK_P	CSI1 clock

The table below shows the combinations of camera usage for different use cases.

Table 3.8-13 MIPI CSI Camera Use Cases

CSI PHY	Use case	Comment
CSI0	Up to 4 lane	One Camera of 4 lane or One camera of 3 lane One Camera of 2 lane One Camera of 1 lane
CSI 1	Up to 4 lane	One Camera of 4 lane or One camera of 3 lane One Camera of 2 lane One Camera of 1 lane
CSI 2	Up to 4 lane	One Camera of 4 lane or 2 x Camera of 1 lane each
CSI0 + CSI1	Up to 4 lane 3D	4 lane 3D use case / Dual 4 lane configuration
CSI 2	Up to 1 lane 3D	1 lane 3D use case / Dual 1 lane configuration
CSI0 + CSI1 + CSI2	Up to 4 lane	Three 4-lane CSI (4+4+4 or 4+4+2+1)
CPHY		Three 3-trio CPHY1.0

3.8.3 Vertigo Sensor connector

The HDK development kit supports a 30-pin connector (449-53935-0030) to support Vertigo 10 or follow on card.

Vertigo 10 sensor card is designed and managed by the Qualcomm sensor team.

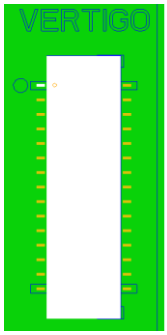

Figure 3-21 Vertigo Connector (J1701)

3.8.4 HDMI Connector

The HDMI type A connector enables the HDK development platform to connect to an external HDMI monitor/ television via an HDMI cable. The HDK supports HDMI output up to 1920x1080. The LT9611 MIPI DSI to HDMI1.4 bridge IC itself features a resolution up to 4K30Hz.

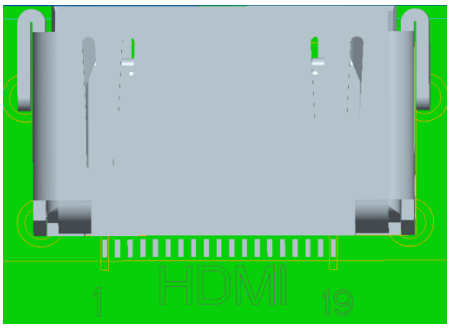

Figure 3-22 HDMI Connector (J1401)

A dip switch, which is DSI1_SW_SEL(S2301-8), provides an option to boot with on-board display or external HDMI monitor/television. The switch should be set before device power on and the default setting is for display. (off = display; on=HDMI)

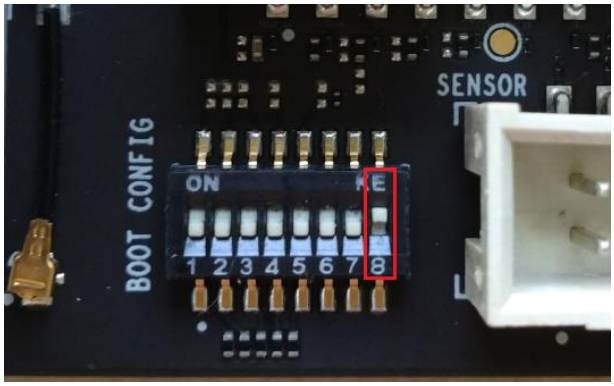

Figure 3-23 Dip Switch S2301-8

See **Table 3.8-2 Dip Switch S2301 HW / SW configuration** for more details.

To disable UEFI display before using HDMI, run the following command:

fastboot oem select-display-panel none

3.9 Display Card

Table 3.9-1 Display Card Mechanical Properties

Dimensions	61.48cm^2 (106mm x 58 mm)
Major Interfaces	one 100-pin high speed board-to-board connector

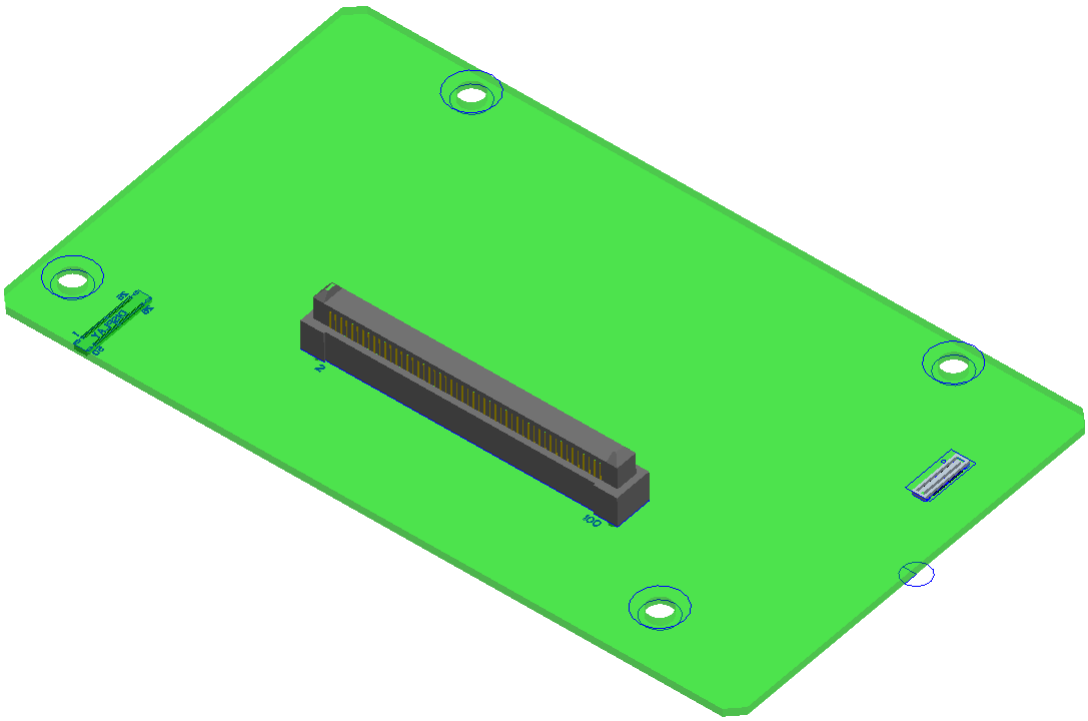

Figure 3-24 HDK 670 Display Card

3.9.1 Display Card Overview

The display output options for the HDK670 Development Kit consists of A 100-pin display connector J0501 that supports:

- Dual DSI DPHY 1.2
- Touch screen capacitive panels via I2C, SPI, and interrupts (up to two devices)
- Backlight LED
  - Can support external backlight driver control and power
  - PM670 Triple supply topology for TFT display panels

The development platform can support the following display combination

MIPI DSI	1 x 4lane DSI0 Support up to FHD+ (2160 x 1440) at 60fps

3.9.2 Display Card Connector J0501

The 100-pin display card connector provides the following features/ pin-outs that enables the development kit to connect to a MIPI DSI panel/ device:

NOTE: Please refer to the carrier schematic and display card tech notes when designing a custom display card.

- DSI
  - 1 x 4 lane DSI
- Backlight
  - Switched-mode boost supply to adaptively boost voltage for series WLEDs with three regulated current sinks
    - Three LED strings (28V OVP) of up to 30 mA each
    - 28V maximum boost voltage
- LCD Display bias supplies
  - Supports a thin film transistor LCD (TFT-LCD) in PM670L
    - 2.8V to 4.75V input voltage range
    - Single inductor LCD bias power supply
    - Independently programmable positive and negative output voltages
      - Positive: 4.0V to 6.0V
      - Negative: -4.0V to -6.0V
- Display connector
  - TFT with integrated backlight
  - TFT with external backlight
- Additional GPIOs for general purposes available
- Touch Panel
  - Supports up to two touch screen controllers
  - Supports I2C or SPI via QUP and SSC_SPI_2
  - Can chose between I2C or SPI signals via MUX

Power specifications:

The display card connector supports the following power domains:

Table 3.9-2 Display Power Domains

Display Signal	Power Domain
PM670 VREG_L11A (1.8V)	up to 150 mA
PM670 VREG_L3B (3.0V)	up to 600 mA
PM670 VREG_L13A (1.8V)	up to 600 mA
Carrier 3.3V	up to 0.5A
Carrier 5 V	up to 1.5A
Carrier 12 V	up to 0.5A

The HDK670 display card is an additional PCBA that mates with the display connector J1301 on the carrier board. This board allows users to interface with the development kit via the LCD that comes preinstalled on the display card. Table 3.9-2 illustrates the interfacing connectors on the display card.

3.9.2.1 Connecting the Display Card to the Development Kit

This configuration allows the user to use the preinstalled LCD display that comes with the display board. As shown in the block diagram below, the MIPI DSI0 lines, which come from the 100-pin ERM8 connector, directly connects to the TFT panel. See the section below for more details on this LCD panel. It is important to note that connector J0501 of the display card needs to connect to J1301 of the carrier board for this configuration to work.

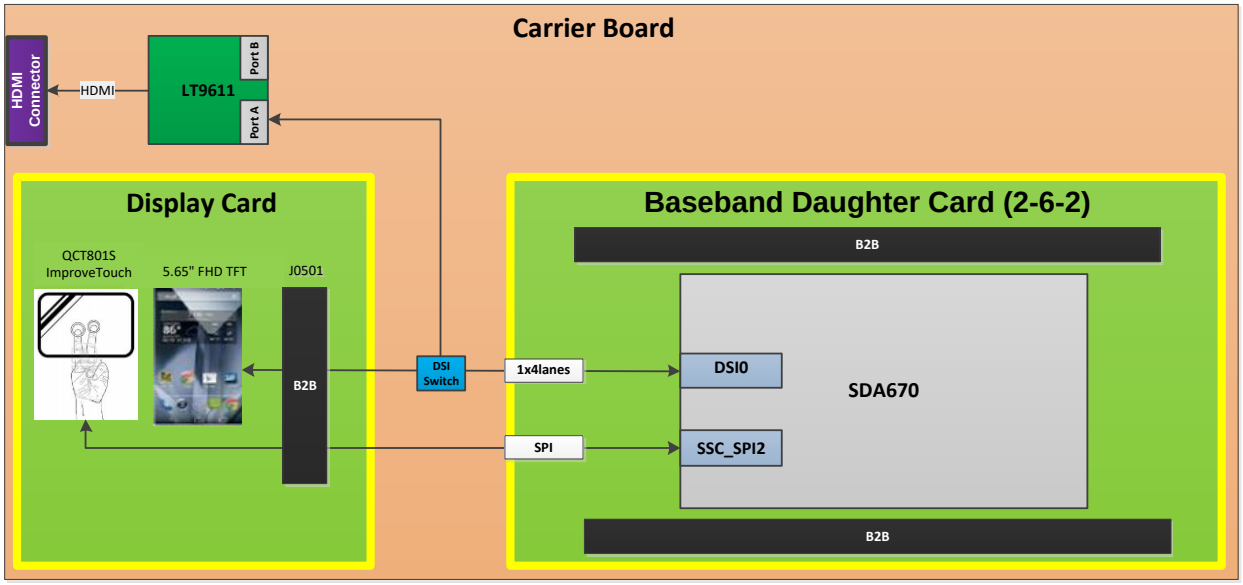

Figure 3-25 Display Card Default Configuration

3.9.3 Display panel

This LCD panel comes preinstalled on the HDK670 display card. Below are the Panel specifications:

- Resolution: FHD+ 2160x1440
- LCD Type: TFT
- PCAP touch panel
- Number of Lanes: 1 x 4 lane MIPI DSI interface via Display Card
- Diagonal Length: 5.65”