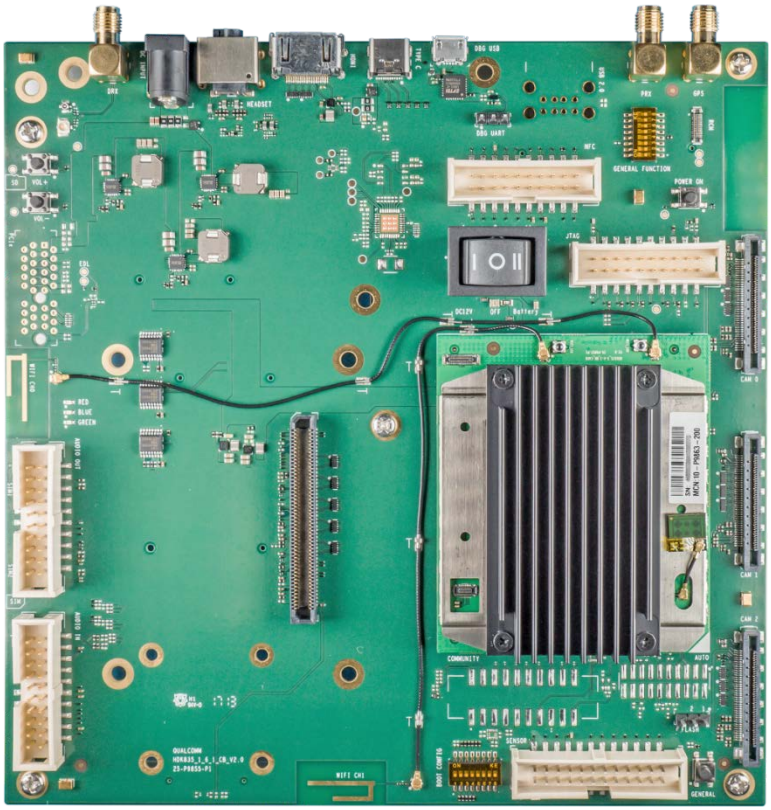

Open-Q™ 835 Development Kit based on the Snapdragon™ 835 (APQ8098) Processor User Guide

[Document: ITC-01IMP1283-UG-001 Version: 1.0]

IDENTIFICATION

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1.0	May 10, 2017	Initial Draft	All

Table of Contents

1. INTRODUCTION

1.1 Purpose

The purpose of this user guide is to provide primary technical information on the Open-Q™ 835 Development Kit based on the Snapdragon™ 835 (APQ8098) Processor.

For more background information on this development kit, visit: www.intrinsyc.com

1.2 Scope

This document will cover the following items on the Open-Q 835 Development Kit:

- Block Diagram and Overview
- Hardware Features
- Configuration
- Processor board
- Carrier Board
- Display Board for LCD (Optional)

1.3 Intended Audience

This document is intended for users who would like to develop custom applications on the Intrinsyc Open-Q 835 Development Kit.

2. DOCUMENTS

This section lists the supplementary documents for the Open-Q 835 Development Kit.

2.1 Applicable Documents

REFERENCE	TITLE
A-1	Intrinsyc Purchase and Software License Agreement for the Open-Q Development Kit

2.2 Reference Documents

REFERENCE	TITLE
R-1	Open-Q 835 Schematics (Processor board, Carrier)

2.3 Terms and Acronyms

Term and acronyms	Definition
AMIC	Analog Microphone
ANC	Audio Noise Cancellation
B2B	Board to Board
BLSP	Bus access manager Low Speed Peripheral (Serial interfaces like UART / SPI / I2C/ UIM)
BT LE	Bluetooth Low Energy
CSI	Camera Serial Interface
DSI	MIPI Display Serial Interface
EEPROM	Electrically Erasable Programmable Read only memory
eMMC	Embedded Multimedia Card
FCC	US Federal Communications Commission
FWVGA	Full Wide Video Graphics Array
GPS	Global Positioning system
HDMI	High Definition Media Interface
HSIC	High Speed Inter Connect Bus
JTAG	Joint Test Action Group
LNA	Low Noise Amplifier
MIPI	Mobile Industry processor interface
MPP	Multi-Purpose Pin
NFC	Near Field Communication
RF	Radio Frequency
SATA	Serial ATA
SLIMBUS	Serial Low-power Inter-chip Media Bus
SPMI	System Power Management Interface (Qualcomm® PMIC / baseband proprietary protocol)
SSBI	Single wire serial bus interface (Qualcomm® proprietary mostly PMIC / Companion chip and baseband processor protocol)

UART	Universal Asynchronous Receiver Transmitter
UFS	Universal Flash Storage
UIM	User Identity module
USB	Universal Serial Bus
USB HS	USB High Speed
USB SS	USB Super Speed

2.4 List of Figures

2.5 List of Tables

3. OPEN-Q 835 DEVELOPMENT KIT

3.1 Introduction

The Open-Q 835 Development Kit provides a quick reference or evaluation platform for Qualcomm's latest 835 series - Snapdragon™ 835 processor. This kit is suited for Android / Linux application developers, OEMs, consumer manufacturers, hardware component vendors, video surveillance, robotics, camera vendors, and flash chip vendors to evaluate, optimize, test and deploy applications that can utilize the Qualcomm® Snapdragon™ 835 series technology.

3.2 Development Platform Notice

This development platform contains RF/digital hardware and software intended for engineering development, engineering evaluation, or demonstration purposes only and is meant for use in a controlled environment. This device is not being placed on the market, leased or sold for use in a residential environment or for use by the general public as an end user device.

This development platform is not intended to meet the requirements of a commercially available consumer device including those requirements specified in the European Union directives applicable for Radio devices being placed on the market, FCC equipment authorization rules or other regulations pertaining to consumer devices being placed on the market for use by the general public.

This development platform may only be used in a controlled user environment where operators have obtained the necessary regulatory approvals for experimentation using a radio device and have appropriate technical training. The device may not be used by members of the general population or other individuals that have not been instructed on methods for conducting controlled experiments and taking necessary precautions for preventing harmful interference and minimizing RF exposure risks. Additional RF exposure information can be found on the FCC website at http://www.fcc.gov/oet/rfsafety/

3.3 Anti-Static Handling Procedures

The Open-Q 835 Development Kit has exposed electronics and chipsets. Proper anti-static precautions should be employed when handling the kit, including but not limited to:

- Using a grounded anti-static mat
- Using a grounded wrist or foot strap

3.4 Kit Contents

The Open-Q 835 Development Kit includes the following:

- Open-Q 835 Processor board with the Snapdragon™ 835 (APQ8098) processor main CPU board
- Mini-ITX form-factor carrier board for I/O and connecting with external peripherals
- GNSS Card
- 5.5” Full HD (1440x2560) AMOLED Display card (Additional Accessory)
- AC power adapter

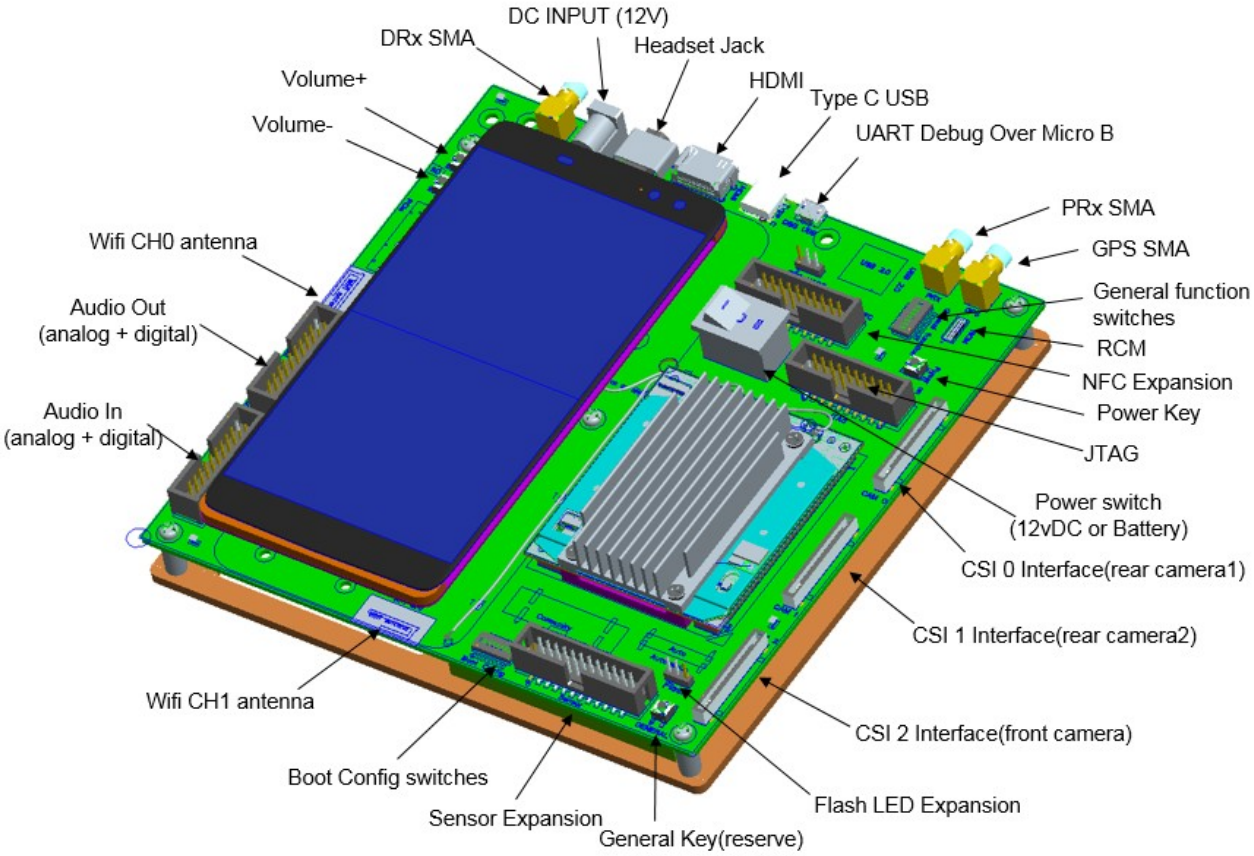

Figure 1 Assembled Open-Q 835 Development Kit TOP

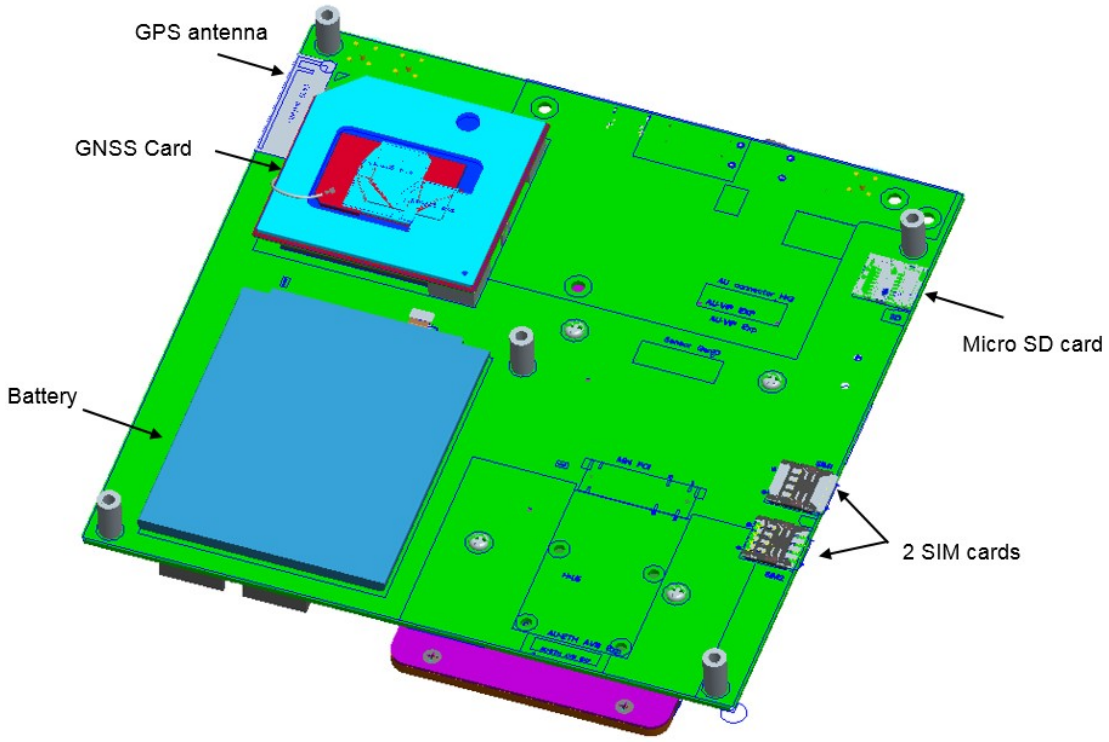

Figure 2 Assembled Open-Q 835 Development Kit BOT

The development kit comes with Android software pre-programmed on the CPU board or processor board. Please contact Intrinsyc for availability of camera modules, sensor boards, and other accessories: sales@intrinsyc.com

3.5 Hardware Identification Label

Labels are present on the CPU board. The following information is conveyed on these two boards:

Processor board:

- Serial Number
- WIFI MAC address

Refer to http://support.intrinsyc.com/account/serialnumber for more details about locating the serial number, as this will be needed to register the development kit. To register a development kit, please visit: http://support.intrinsyc.com/account/register

Note: Please retain the and carrier board serial number for warranty purposes.

3.6 System Block Diagram

The Open-Q 835 development platform consists of three major components

- Open-Q 835 Processor board
- Carrier board for I/O and connecting with external peripherals
- GNSS Card
- Display Adapter Board (additional accessory)

The following diagram explains the interconnectivity and peripherals on the development kit.

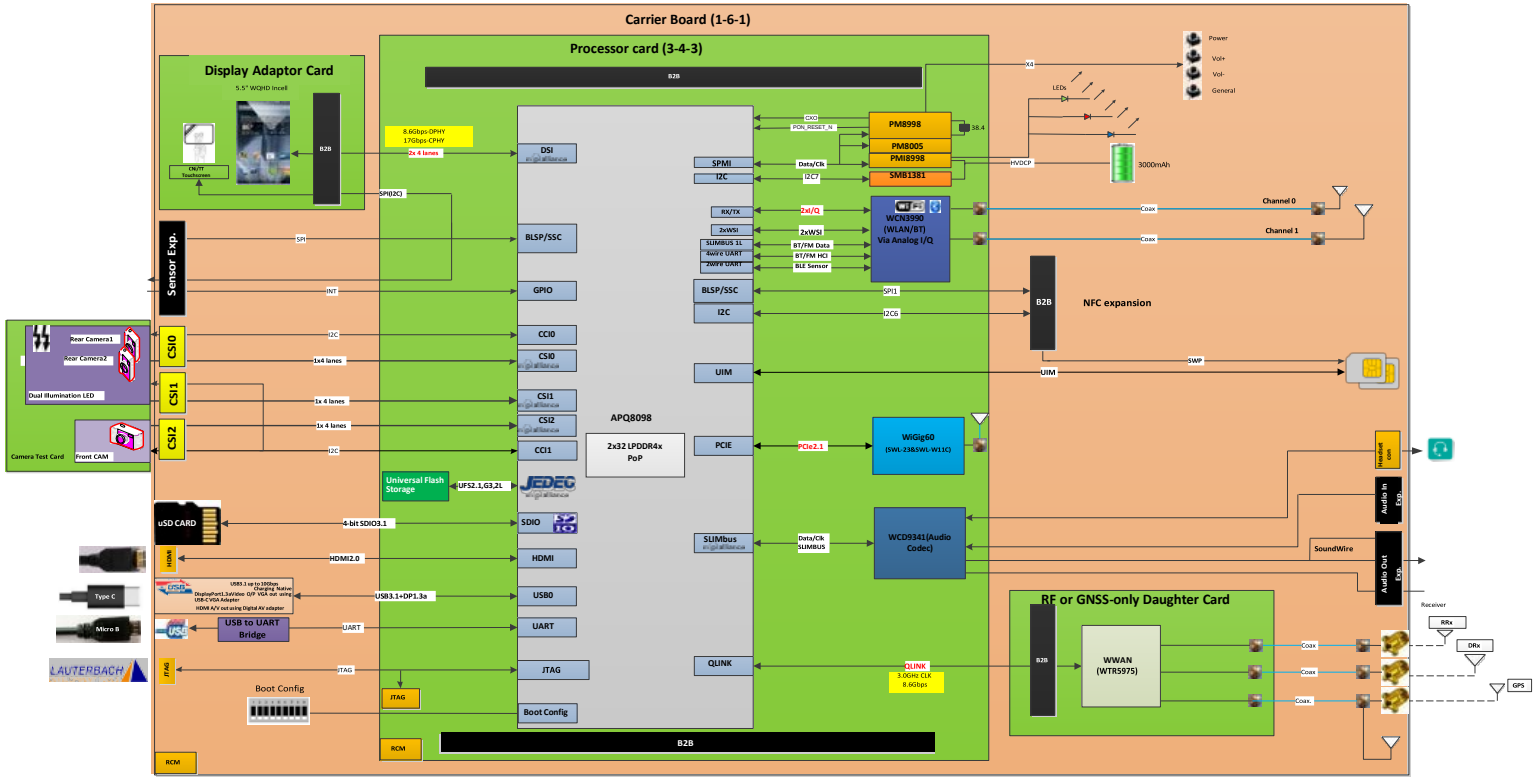

Figure 3 Open-Q 835 Processor board + Carrier Board Block Diagram

3.7 Open-Q 835 Processor Board

The Processor board provides the basic common set of features with minimal integration efforts for end users.

It contains the following:

- Snapdragon™ 835 (APQ8098) main application processor
- LPDDR4 up to 1866MHz 4GB RAM (POP)
- PMI8998 + PM8998 – PMIC for Peripheral LDOs, Boost Regulators
- WCN3990 Wi-Fi + BT +FM combo chip over SLIMbus, Analog IQ, UART, PCM
- 128 GB UFS 2.1.
- WCD9341 Audio Codec

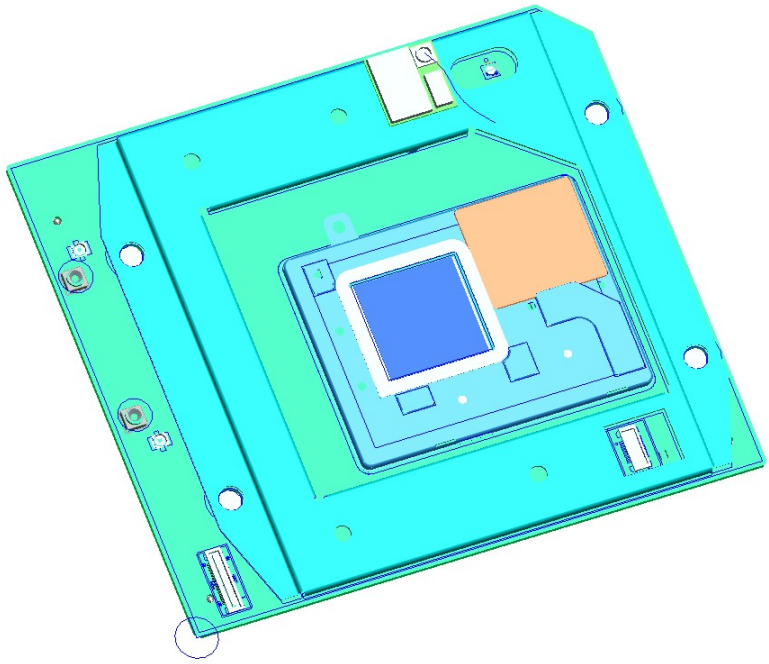

Figure 4 Open-Q 835 PROCESSOR BOARD

3.7.1 Processor Board Mechanical Properties

Table 3.7-1 Open-Q 835 Processor Board Mechanical Properties

Area	42 cm^2(60 mm x 70 mm)
Interface	2 x 240-pin high speed board to board connectors.
Thermal	A top side heat sink and a bottom side heat conductive metal plate are installed by default.

3.7.2 Processor Board Block Diagram

The Open-Q 835 Processor board measuring 60mm x 70mm is where all the processing occurs. It is connected to the carrier board via two 100 pin Hirose 240-pin connectors. The purpose of these connectors is to bring out essential signals such that other peripherals can be connected to the platform.

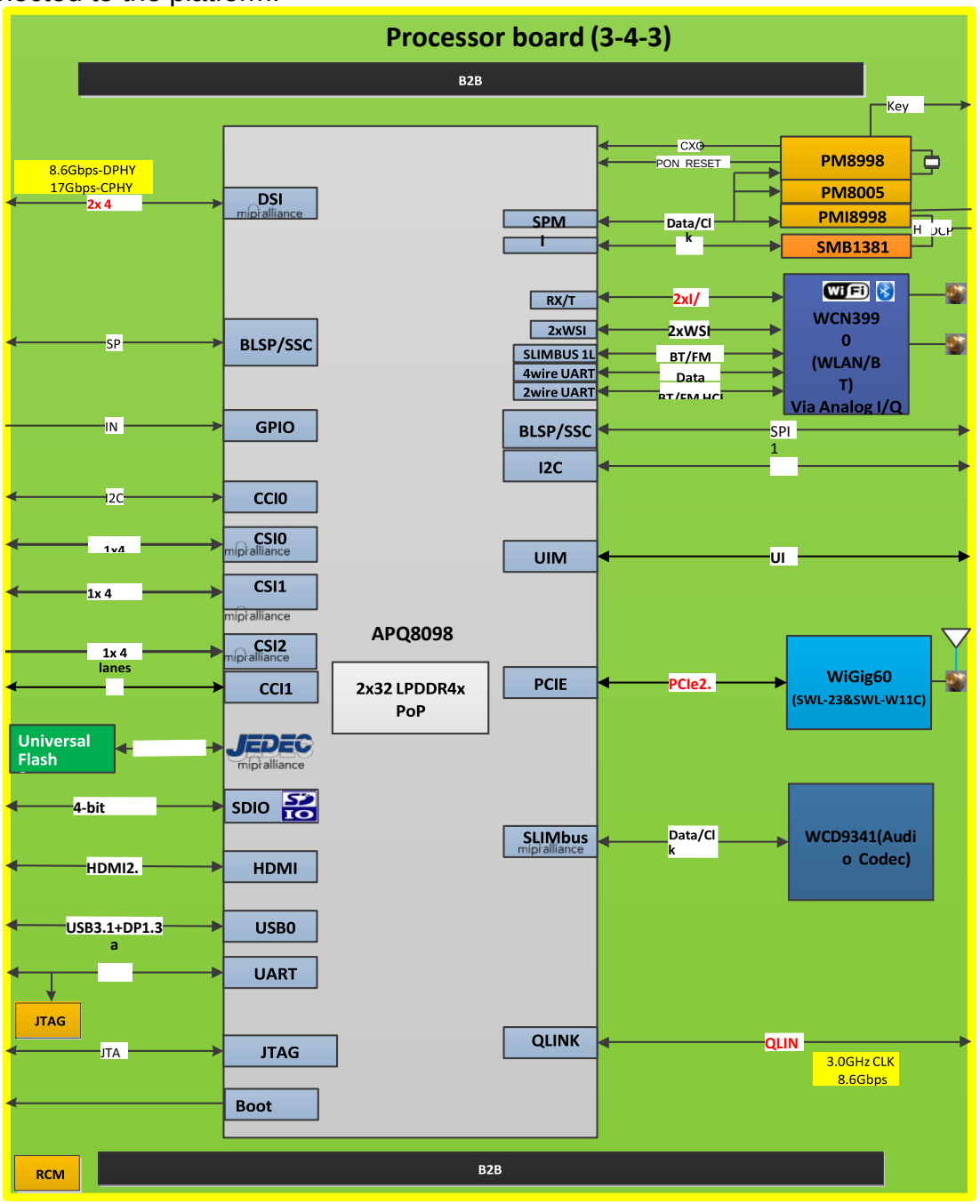

Figure 5 Open-Q 835 Processor Board Block Diagram

3.7.3 Hardware Specification

The Open-Q 835 Processor Board platform encompasses the following hardware features:

Table 3.7-2 Open-Q 835 Processor Board Hardware Features

Subsystem / Connectors	Feature Set	Description	Specification
Chipset	APQ8098	Qualcomm® Snapdragon™ 835 Processor	Qualcomm® Kyro CPU, quad core, 64-bit ARM V8 compliant processor, 2.2GHz
	PMIC (PM8998 & PMi8998)	Qualcomm® PMIC, Companion PMIC for APQ8098 processor	NA
Memory	4GB LPDDR4	Memory POP	Up to 1866MHz LPDDR4 POP on CPU BGA chip. Supports via 2x32bit channels
	32 GB UFS	Primary Storage for platform. Mainly used for storing SW applications and user data etc.	Toshiba UFS on board. Can support up to 128GB
Connectivity	Wi-Fi 2.4 GHz/ 5GHz via WCN3990 – Analog IQ, WSI 2.0	WCN3990 Wi-Fi + BT +FM Combo Chip	802.11a/b/g/n/ac 2.4/5.0 GHz via WCN3990 over analog IQ, WSI 2.0, Full 2x2 antenna configuration
	BT 2.4 GHz via WCN3990 – UART / SLIMbus	WCN3990 Wi-Fi + BT +FM Combo Chip	Support BT 5.0 + HS and backward compatible with BT 1.x, 2.x + EDR
	GNSS via WTR5975 – Qlink Qualcomm Proprietary Protocol	GNSS Frontend	GPS/ GLONASS/ COMPASS/Galilei
RF Interfaces	2xWLAN / BT	Connect to antenna on carrier board via coax cable	2.4 / 5 GHz
	1x GNSS	Connect to antenna on carrier board via coax cable	GPS/ GLONASS/ COMPASS /Galilei
Audio	1 x Headset Output	Headset/ headphone output	Analog differential output
	2 x Loud-speaker	2 x loud-speaker output	Digital output
	1 x Earpiece output	Earpiece output	Analog differential output
	3 x analog MICs	Analog MIC input	Analog differential input
	3 x digital MICs	Digital MIC input	Digital input
Camera	3 x MIPI CSI	Camera Connectors CSI0, CSI1, CSI2	MIPI Alliance Specification v1.2
Display	1 x MIPI DSI (DSI0 & DSI1) + Touch 100-pin display Connector	100- pin display connector.	MIPI Alliance Specification v1.2. MIPI D-PHY Specification v0.65, v0.81, v0.90, v1.01, v1.2
USB	1 x USB HS 1 x USB SS	1 x Type-C USB 3.1	USB3.1
PCIe	1 X PCIe	PCIe 0 PCIe signal to Wigig module. Reserve option for PCIe SLOT1 and MiniPCIe(hardware rework is needed)	PCI Express Specification, Rev 2.1
Connectors	2 x 240pin BB Card	Connector for BB Card	2 x 240 pin B2B connector

Subsystem / Connectors	Feature Set	Description	Specification
	connector		

3.7.4 Processor Board RF Specification for WIFI, BT

The Processor board includes the following radio interfaces:

- Wi-Fi + BT: WiFi CH0
- Wi-Fi only: WiFi CH1
- WTR5975: For GNSS RF Front end

Antenna 0: Antenna 0 is the primary interface for WCN3990 to provide Wi-Fi connectivity and Bluetooth connectivity. This antenna connector is connected to carrier board PCB antenna via a coaxial cable. ANT0 is a standard dual band antenna from 2.4 GHz to 5 GHz and BT.

Antenna 1: Antenna 1 is for WCN3990 to provide Wi-Fi. Antenna connector ANT1 is connected to the carrier board antenna via a coaxial cable. The function of this connector is for extending the dual band capabilities of the Wi-Fi chip; therefore, enabling this antenna to be used simultaneously with Antenna 0. For example, Antenna 0 can be connected to 2.4GHz while Antenna 1 can be connected to 5 GHz.

For details on connecting the WiFi module to the on-board PCB antennas on the carrier board, refer to section 0 below.

For GNSS details, See section **3.8.23 GNSS Card**

3.8 Open-Q 835 Carrier Board

The Open-Q 835 Carrier board is a Mini-ITX form factor board with various connectors used for connecting different peripherals. The following are the mechanical properties of the carrier board:

Table 3.8-1 Open-Q 835 Carrier Board Mechanical Properties

Dimensions	289 cm^2 (170mm x 170mm)
Form Factor	Mini-ITX
Major Interfaces	BB Card: 2x240 pin board to board connector Display: 100 pin board to board connector GNSS: 2x240 pin board to board connector
Thermal	Thermal pad is placed between the BB card and carrier board

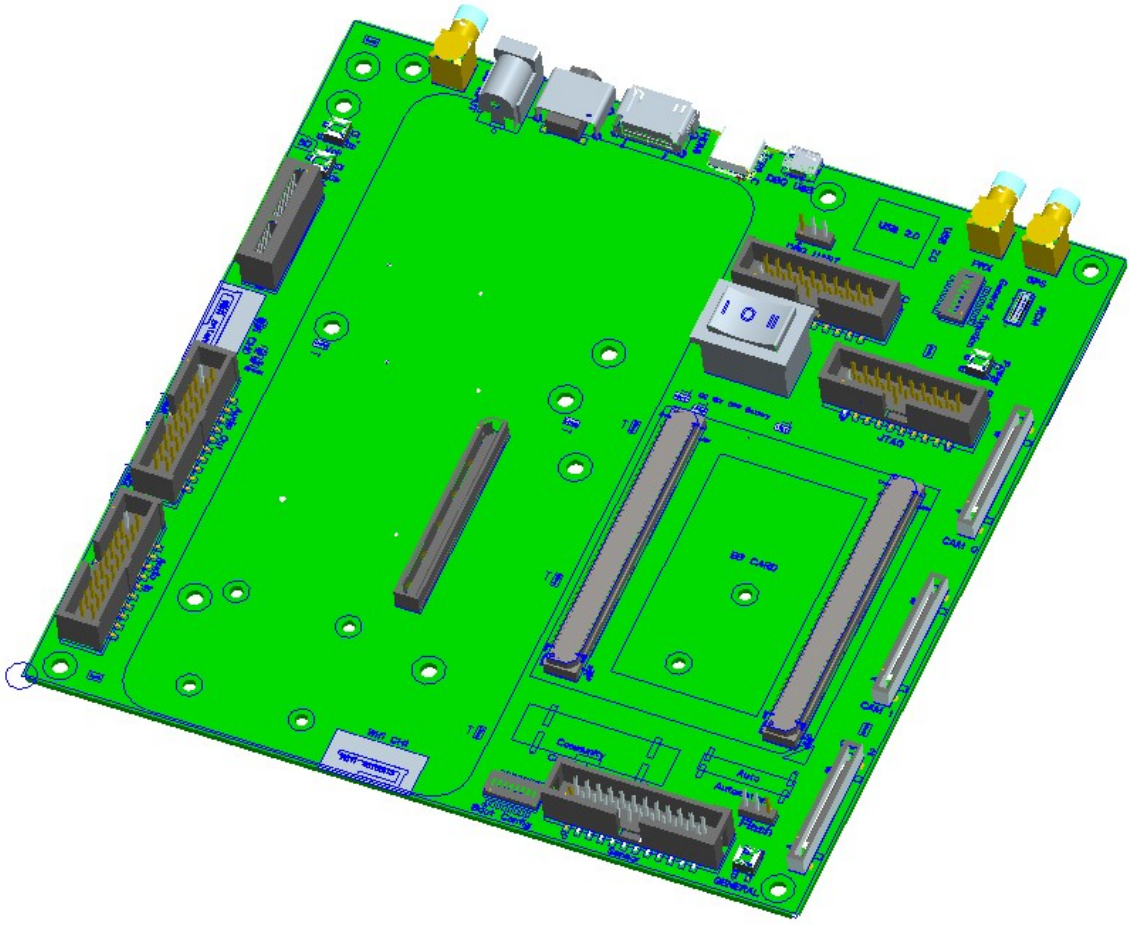

Figure 6 Open- Q™ 835 Carrier Board

3.8.1 Dip switch S10 Configuration Options

There is a DIP switch S2301 on the south top side of the Open-Q 835 carrier board. The 8-bit switch allows the user to control the system configuration and boot options. Table 3.8-1 below outlines the pin outs and connections of this DIP switches.

Table 3.8-2 Dip Switch S2301 HW / SW configuration

Function	DIP Switch	Description	Notes
FORCED_USB_BOOT	S2301-1	Toggles between FORCE USB boot and EDL mode. Enables FOCE USB (GPIO 57) when DIP switch turned on	Default out of the box configuration is OFF
WATCHDOG _DISABLE	S2301-2	Enables WATCHDOG_DISABLE when DIP switch turned on. Controlled by APQ- GPIO 101	Default out of the box configuration is OFF
BOOT_CONFIG[1]	S2301-3	Enables APQ boot configuration 1 when DIP switch turned on. Controlled by APQ-GPIO102	Default out of the box configuration is OFF
BOOT_CONFIG[2]	S2301-4	Enables APQ boot configuration 2 when DIP switch turned on. Controlled by APQ-GPIO103	Default out of the box configuration is OFF
BOOT_CONFIG[3]	S2301-5	Enables APQ boot configuration 3 when DIP switch turned on. Controlled by APQ- GPIO104 See schematic for boot configuration options.	Default out of the box configuration is OFF
N/C	S2301-6	NA	NA
N/C	S2301-7	NA	NA
N/C	S2301-8	NA	NA

There is another DIP switch S2302 on the north top side of Open-Q 835 carrier board. The 8-bit switch allows the user to control the system configuration and boot options. Table below outlines

Table 3.8-3 Dip Switch S2303 HW / SW configuration

Function	DIP Switch	Description	Notes
CHARGE_DISABLE	S2302-1	Disable charge when DIP switch turned on	Default out of the box configuration is OFF which enables system charge from USB **Note:** make sure turn on this switch when DC-12V input and USB are both present
N/C	S2302-2	NA	NA
HUB_RESET_SW	S2302-3	Enables hardware reset from general switch(J2204) when DIP switch turned on	Default out of the box configuration is OFF **Note:** Default HUB reset control is from s/w, hardware rework is needed to enable this function
MSM_PS_HOLD	S2302-4	Enables the JTAG_PS_HOLD mode when DIP switch turned on	Default out of the box configuration is OFF
N/C	S2302-5	NA	NA
DISP_IFC_CONFIG	S2302-6	Config the signals connected to DISP_IFC[0:3]	Default out of the box configuration is OFF **Note:** LCD IF is routed to DISP[0:3] by default
AU/NFC_SPI_CONFIG	S2302-7	Switch the SPI between AU and NFC	Default out of the box configuration is OFF **Note:** SPI is routed to NFC by default
BLSP_TP_CONFIG	S2302-8	Config the signals connected to BLSP_TP	Default out of the box configuration is OFF **Note:** BLSP5 is routed to BLSP_TP by default

Warning! : Before making any changes to the dip switch, make sure to note down the previous configuration. The default switch settings are above.

3.8.2 Carrier Board Expansion Connectors

The following table lists the connectors, expansions and their usages on the carrier board:

Table 3.8-4 Carrier Board Expansion Options and Usage

Domain	Description	Specification	Usage
Power	AC / Barrel charger	12 V DC Power Supply 5 A	Power Supply
	Battery connector	8 pin header	For providing power from 4.35V/3000mAh battery
Debug Serial via USB	Debug Serial UART console over USB for development	USB Micro B connector	Development Serial Connector for debug output via USB
JTAG	OS / Firmware /QFROM Programming / Debugging JTAG	Standard 20-pin connector, ARM and OpenDSP – Lauterbach	QFROM / eMMC / Platform EEPROM programming ARM /Open DSP debugging
Buttons	General Purpose	SMD Button	Reserved button for general purpose
	Power	SMD Button	Power Button for Suspend / Resume and Power off
	Volume +	SMD Button	Volume + Key
	Volume –	SMD Button	Volume – Key
NFC Board Header	20 pin NFC expansion connectors	NA	NA
3-Digital Microphone via audio input expansion header	Audio expansion Supported using WCD9341	Digital Audio header	For Digital audio input for Digital MIC, I2S codec, Slim bus interface.
3-Analog Microphone via audio input expansion header	Audio expansion Supported using WCD9341	Analog Audio header	For Analog audio input for Analog MIC (differential signal)
2-Loud Speaker via audio output expansion header	Audio expansion Supported using WCD9341	Analog Audio header	For loud speaker output after signal has been processed
Earpiece via audio output expansion header	Audio expansion Supported using WCD9341	Analog Audio header	For earpiece output after signal has been processed
HDMI Port	Extended Display ports	HDMI port supports up to 4K without HDCP 2.0A spec	External Display
USB 3.1	USB 3.1	Type-C header	Transfer data to and from CPU
WLAN Antenna	2X PCB Antenna	2.4 – 5 GHz	Antenna to BB card
GNSS Antenna	PCB Antenna	GPS: 1574.42 MHz – 1576.42 MHz GLONASS: 1587 MHz – 1606 MHz COMPASS: 1559.05 to 1563.14MHz Galilei: 4.092MHz BW(centered on 1575.42MHz)	Antenna to GNSS module
LED	3xLED	Red: PMIC Driven Green: PMIC Driven	Red: General purpose Green: General purpose

Domain	Description	Specification	Usage
		Blue: PMIC Driven	Blue: General purpose
LCD Display and Touch connector	100 pin for LCD signals from B2B boards for display	4-lane MIPI DSI0, DSI1, I2C/SPI/GPIO Backlight MIPI Alliance Specification v1.2 MIPI D-PHY Specification v0.65, v0.81, v0.90, v1.01, V1.2 MIPI C-PHY Specification v1.0	Can work as one dual DSI or both independent display
Sensor header	24 pin sensor header	24 pin sensor header	Header to connect sensor board.
SIM Card	WWAN SIM card connector (optional)	4bit Micro SIM card support	For WWAN mini PCI express cards (for internal use only – not supported)
CSI Camera connectors	3 x CSI port connector with CLK, GPIOS, CCI	Supports 3 x Camera interfaces via three separate connectors ▪ 3 x MIPI-CSI each 4 lane ▪ External flash driver control ▪ Support for 3D camera configuration ▪ Separate I2C / CCI control MIPI Alliance Specification v1.2 for Camera Serial Interface	
RCM Header	20 pin RCM header	Sense lines connected across 0.01 Ohm resistor	To measure system current consumption (for internal use only))

The sections below will provide in depth information on each expansion header and connector on the carrier board. The information listed below is of particular use for those who want to interface other external hardware devices with the Open-Q 835 Processor board. Before connecting anything to the development kit, please ensure the device meets the specific hardware requirements of the processor.

3.8.3 DC Power Input J0701

The Open-Q 835 Development Kit power source connects to the 12V DC power supply jack J0701. Starting from the power jack, the 12V power supply branches off into different voltage rails via step down converters on the carrier board and PMIC on the Processor board. The Processor board is powered by 3.8V via a Silergy step down converter U0703 on the carrier board. To ensure the Processor board is getting powered correctly, user can monitor the current going into the Processor board via the power probe header J0901 (see section below).

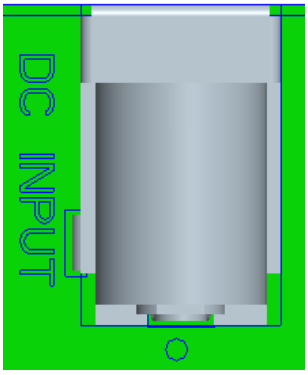

Figure 7 J0701 12V DC Power Jack

The Processor board has 2 PMIC modules. Functionalities of the 2 modules are outlined below.

PMI8998 PMIC is used for:

- Source various regulated power rails
- Battery charging. Please see section below for additional information on battery support. A DIP S2302A switch is used to enable/disable charge function. Make sure turn off battery charging when 12V DC in is used and USB charger is inserted.
- Please note that support for battery charging over external charger is not implemented in the design. Please contact Intrinsyc for such customization.

PM8998 PMIC is used for:

- Source various regulated power rails
- Source system clock

3.8.4 Battery Header J1001

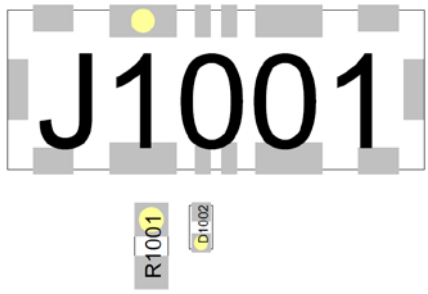

Figure 8 J1001 Battery Header

The Open-Q 835 development platform can also power the Processor board with a single cell Lithium-Ion Polymer (LiPo) battery pack which connects to header J1001. The purpose of this header is to be used by the end user to develop a battery charging solution, including battery characterization. Intrinsyc recommends using the single cell Lithium ion battery pack that is available with the development kit. If user intends to use a different battery, please note the pin outs on this battery header.

Table 3.8-5 J1001 Battery Header Pin out

Description	Signal	Pin	Note
Processor board Battery negative supply terminal	VBAT Minus(VBAT-)	J1001[1]	
NC	NC	J1001[2]	
Internal battery pack temperature	BATT_THERM (The recommended battery has a 10K Ohm thermistor)	J1001[3]	
Processor board Battery positive supply terminal	VBAT Plus (VBAT+)	J1001[4]	
Processor board Battery positive supply terminal	VBAT Plus (VBAT+)	J1001[5]	
Processor board Battery positive supply terminal	VBAT Plus (VBAT+)	J1001[6]	
	BATT_ID	J1001[7]	
Processor board Battery negative supply terminal	VBAT Minus(VBAT-)	J1001[8]	

Please note that the battery only powers the Processor board. To ensure proper functionality of the development kit, the 12V power supply must be attached at J0701. A Dip switch J1003 is used to switch the power source of Processor board between battery and 12V power supply. When a battery is not in use, The Processor board is powered by 3.8V via a Silergy step down converter U0703 on the carrier board .

3.8.5 RCM Header J0901

The RCM header is used to sense/ monitor the current on the 3.8V power rail going into the Processor board. The table below summarizes the pin outs of header J0901.

Table 3.8-6 J10901 Pin out

Description	Signal	Pin
Processor board power positive current sense line	SOM_PWR_SENSE_P	J0901[1]
Processor board power negative current sense line	SOM_PWR_SENSE_N	J0901[2]
GND	GND	J0901[31-34]

3.8.6 Debug Serial UART Header J2103

Figure 9 J2103 Debug UART Header

The UART header and supporting circuitry does not come preinstalled. To have access to the debug UART, a 3-pin header needs to be installed as well as the supporting circuitry. Please see the carrier board schematic for details on what to install for this header to be functional.

The header consists of TX, RX and GND pins. It is a 3.3V TTL UART header. To get the serial terminal working with a PC, the following cable (or similar) is needed

http://www.digikey.ca/product-detail/en/TTL-232R-RPI/768-1204-ND/4382044

Table 3.8-7 J2103 Debug UART Header Pin out

Description	Signal	Pin	FTDI RPI cable connection
APQ UART RX (GPIO5)	BLSP8_UART_RX	J2103[1]	Orange
APQ UART TX (GPIO4)	BLSP8_UART_TX	J2103[2]	Yellow
GND	GND	J2103[3]	Black

3.8.7 Debug Serial UART over USB J2102

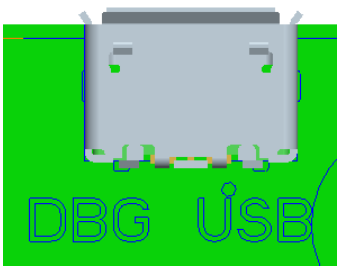

Figure 10 J2102 Debug UART over USB

The UART connection used on the Open-Q 835 is a USB micro B connector (J2102). This debug UART is available over USB via the FTDI FT232RQ chip on the carrier board. To get the serial terminal working with a PC, user needs to ensure that the appropriate FTDI drivers are installed.

3.8.8 JTAG Header J2101

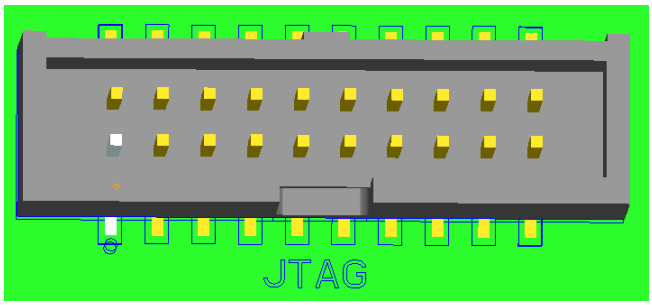

Figure 11 J2101 JTAG Header

This connector provides a JTAG interface to the main processor by which users can connect a JTAG (Lauterbach / USB Wiggler) 20 pin ARM JTAG.

NOTE: It does not provide software support for JTAG

Table 3.8-8 J2101 JTAG Header Pin out

Description	Signal	Pin NO	Description	Signal	Pin NO
GND	GND	J2101[2]	JTAG Power detect	JTAG_PWR	J2101[1]
GND	GND	J2101[4]	Target RESET_N signal	TRST_N	J2101[3]
GND	GND	J2101[6]	TDI Signal (Target DATA IN)	TDI	J2101[5]
GND	GND	J2101[8]	TMS Signal	TMS	J2101[7]
GND	GND	J2101[10]	TCK Signal	TCK	J2101[9]
GND	GND	J2101[12]	JTAG_RTCK signal	JTAG_RTCK	J2101[11]
GND	GND	J2101[14]	TDO Signal (Target Data Out)	TDO	J2101[13]
GND via 4.7KΩ pull down	GND	J2101[16]	Source RESET_N signal	SRST_N	J2101[15]
GND	GND	J2101[18]	NC	NC	J2101[17]
JTAG detect N signal	DET_N	J2101[20]	GND via 4.7KΩ pull down	GND	J2101[19]

3.8.9 Sensor IO Expansion Header J2501

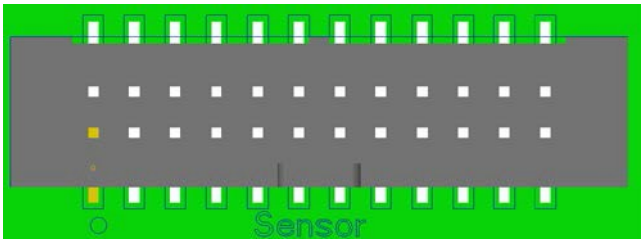

Figure 12 J2501 Sensor Expansion Header

The sensor expansion header J2501 allows for a 24-pin connection to an optional sensor board. If user application does not require a sensor, then this header can be used for other applications that require I2C or GPIO input and output connections.

Following is the pin out for sensor expansion header J2501.

Table 3.8-9 Sensor Expansion Header J2501 Pin out

Description	Signal	Pin NO	Description	Signal	Pin NO
SSC I2C-3 serial data	SSC_I2C_3_SDA	J2501[1]	Accelerometer interrupt input to processor via GPIO117	ACCEL_INT_N	J2501[2]
SSC I2C-3 serial clock	SSC_I2C_3_SCL	J2501[3]	Cap interrupt input to processor via GPIO123	CAP_INT_N	J2501[4]
Sensor reset signal from processor to sensor via GPIO126	MEMS_RESET_N	J2501[5]	Gyroscope interrupt input to processor via GPIO118	GYRO_INT	J2501[6]
Sensor IO PWR 1.8 V VREG_LVS2A _1P8 power supply regulator (Digital)	SENS_IO_PWR	J2501[7]	Sensor Analog power supply from VREG_L19A 2.85V or 3.3V	SENS_ANA_P WR	J2501[8]
GND	GND	J2501[9]	GND	GND	J2501[10]
HRM interrupt/ configurable GPIO122	HRM_INT	J2501[11]	Touch screen interrupt input from processor via GPIO125	TS_INT0	J2501[12]
SSC SPI-1 chip select 2	SSC_SPI_1_CS1_N	J2501[13]	Alternate sensor interrupt input to processor via GPIO120	ALSPG_INT_N	J2501[14]
MISC GPIO for sensor via GPIO84	APQ_GPIO84	J2501[15]	Digital Compass interrupt input to processor via GPIO119	MAG_DRDY_I NT	J2501[16]

Description	Signal	Pin NO	Description	Signal	Pin NO
NC	NC	J2501[17]	Hall sensor interrupt input to processor via GPIO124	HALL_INT_N	J2501[18]
SSC SPI-1 chip select 1	SSC_SPI_1_CS_N	J2501[19]	SSC SPI-1 data master out/ slave in	SSC_SPI_1_M OSI	J2501[20]
SSC SOI-1 clock	SSC_SPI_1_CLK	J2501[21]	SSC SPI-1 data master in/ slave out	SSC_SPI_1_M ISO	J2501[22]
NC	NC	J2501[23]	SSC power enable	SSC_PWR_E N	J2501[24]

In sum, if sensor application is not needed, this expansion header can provide two full BLSP7 and BLSP5 for UART/ SPI/ I2C/ UIM. Please refer to the schematic and consider the power before connecting anything to this header.

Note that there is an unpopulated Gen-10 connector header (J2502) footprint at the bottom of the carrier board. Install the Samtec (part number: QSH-030-01-L-D-A) connector here if needed.

Figure 13 J2502 Gen-10 Sensor Connector (Samtec QSH-030 series)

3.8.10 NFC Expansion Header J2401

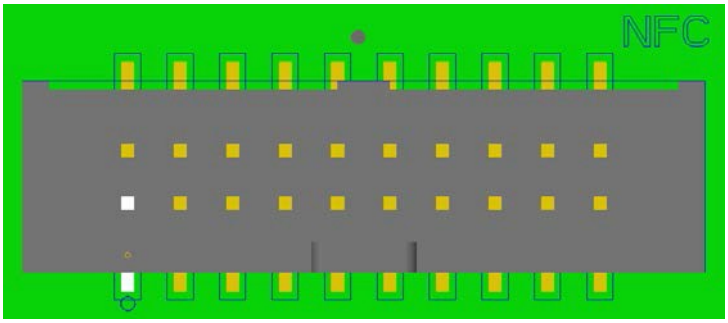

Figure 14 J2401 NFC expansion header

This digital IO expansion header J2401 is a 20 pin connector for attaching an optional NFC board This header also allows user to connect to the free GPIOs and I2C lines when NFC is not used; therefore, enabling other use cases. Please refer to Table below for detailed information regarding the signals that are being brought out by this connector.

Table 3.8-10 NFC Expansion Header J2401 Pin Out

Description	Signal	Pin NO	Description	Signal	Pin NO
BLSP1 bit 0 via APQ GPIO52	NFC_BLSP1_ SPI_CLK	J2401[1]	BLSP1 bit 2 via APQ GPIO50	NFC_BLSP1_ SPI_MISO	J2401[2]
NFC power request GPIO via PM GPIO7	NFC_PWR_REQ	J2401[3]	SIM present GPIO via APQ GPIO112	UIM1_PRESENT	J2401[4]
SIM Card DATA line (UIM1) via APQ GPIO109	UIM1_DATA	J2401[5]	150mA max 3.8V BB CARD power supply pin	BB CARD_SYS_ PWR	J2401[6]
SIM Card Reset line (UIM1) via APQ GPIO111	UIM1_RESET	J2401[7]	NFC interrupt IRQ pin via APQ GPIO106	NFC_IRQ	J2401[8]
SIM CLK line (SIM1) via APQ GPIO110	UIM1_CLK	J2401[9]	NFC Disable signal via APQ GPIO105	NFC_DISABLE	J2401[10]
1.8V Voltage regulator supply max 150mA via PM8998	VREG_L9A_1P8	J2401[11]	BLSP8 I2C Bus-8 I2C SDA line	BLSP8_I2C_SDA	J2401[12]
1.8V Voltage regulator supply max 150mA via PM8998	VREG_S4A_1P8	J2401[13]	BLSP68I2C Bus-8 I2C CLK line	BLSP8_I2C_SCL	J2401[14]
GND	GND	J401[15]	NFC clock request signal via PM GIO10	NFC_CLK_REQ	J2401[16]
PM8998 free running clock via buffer	BBCLK2	J2401[17]	NFC download request via APQ GPIO93	NFC_DWL_REQ	J2401[18]
BLSP1 1 bit via APQ GPIO51	NFC_BLSP1_ SPI_CS_N	J2401[19]	BLSP1 3 bit via APQ GPIO49	NFC_BLSP1_ SPI_MOSI	J2401[20

In general, if there is no need for NFC application, this expansion header can provide two GPIOs, I2C, free running clocks, and enable voltage/ power source to external peripherals.

3.8.11 ANC Headset Jack J1501

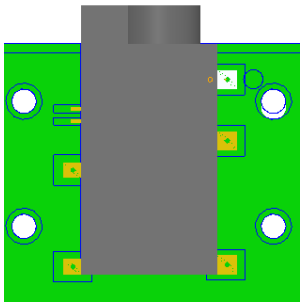

Figure 15 J1501 ANC Headphone Jack

The ANC headset jack (J1501) is a special 3.5mm TRRS jack with ANC capabilities. It is backwards compatible with standard headset jacks. Please contact Intrinsyc at sales@intrinsyc.comfor compatible ANC headsets.

3.8.12 Audio Inputs Expansion Header J1601

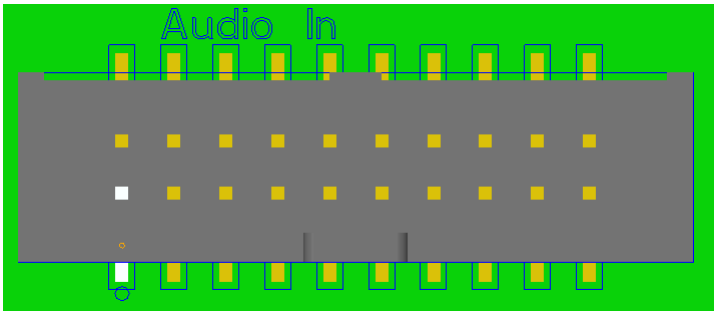

Figure 16 J1601 Audio Inputs Expansion Header

This header expansion provides the following audio inputs:

1. 3 digital mics
2. 3 analog mics
3. Voltage rails to support analog and digital mics

The table below outlines the pin out information of the audio inputs expansion header J1601:

Table 3.8-11 Audio Inputs Expansion Header J1601 Pin out

Description	Signal	Pin NO	Description	Signal	Pin NO
Analog MIC1 positive differential input	CDC_IN1_P	J1601[1]	Analog MIC1 negative differential input	CDC_IN1_N	J1601[2]
Analog MIC3 positive differential input	CDC_IN3_P	J1601[3]	Analog MIC3 negative differential input	CDC_IN3_N	J1601[4]
MIC bias output voltage 1	MIC_BIAS1	J1601[5]	MIC bias output voltage 3	MIC_BIAS3	J1601[6]
Analog MIC4 or MIC5 positive differential input	CDC_IN4/5_P	J1601[7]	Analog MIC4 or MIC5 negative differential input	CDC_IN4/5_N	J1601[8]
MIC bias output voltage 4	MIC_BIAS4	J1601[9]	3.3V power supply max 500mA	MB_VREG_3P3	J1601[10]
GND	GND	J1601[11]	GND	GND	J1601[12]
Clock for digital MIC 1 and 2	CDC_DMIC_CLK0	J1601[13]	Clock for digital MIC 3 and 4	CDC_DMIC_CLK1	J1601[14]
Digital MIC 1 and 2 data line	CDC_DMIC_DATA0	J1601[15]	Digital MIC 3 and 4 data line	CDC_DMIC_DATA1	J1601[16]
1.8V power supply max 300mA	VREG_S4A_1P8	J1601[17]	Clock for digital MIC 5 and 6	CDC_DMIC_CLK2	J1601[18]
GND	GND	J1601[19]	Digital MIC 5 and 6 data line	CDC_DMIC_DATA2	J1601[20]

3.8.13 Audio Outputs Expansion Header J1602

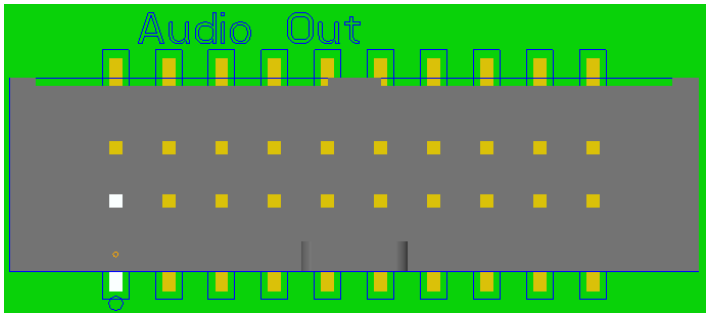

Figure 17 J1602 Audio Outputs Expansion Header

This header expansion provides the following audio outputs:

1. 2 differential analog audio line out
2. 2 single ended analog audio line out
3. 1 differential analog earpiece amplifier output (no external amp needed)
4. 2 speaker amplifier enable control
5. Voltage rails to support analog and digital mics

The table below outlines the pin out information of the audio outputs expansion header J1602:

Table 3.8-12 Audio Outputs Expansion Header J1602 Pin out

Description	Signal	Pin NO	Description	Signal	Pin NO
Analog audio line out 1, positive differential output	LINE_OUT1_P	J1602[1]	Analog audio line out 1, negative differential output	LINE_OUT1_N	J1602[2]
Analog audio line out 2, positive differential output	LINE_OUT2_P	J1602[3]	Analog audio line out 2, negative differential output	LINE_OUT2_N	J1602[4]
Audio line single end outputs GND reference (connect to ground)	LINE_REF	J1602[5]	3.3V output power supply	MB_VREG_3P3	J1602[6]
Analog audio line out 1, single ended output	LINE_OUT1_P	J1602[7]	Analog audio line out 2, single ended output	LINE_OUT2_P	J1602[8]
Analog earpiece amplifier out, positive differential output	CDC_EAR_P	J1602[9]	Analog earpiece amplifier out, negative differential output	CDC_EAR_N	J1602[10]
GND	GND	J1602[11]	3.8V output power supply	MB_VREG_BB CARD	J1602[12]
Digital sound wire data for WSA8810/ WSA8815 smart speaker amplifier	CDC_SWR_ CLK	J1602[13]	Digital sound wire data for WSA8810/ WSA8815 smart speaker amplifier	CDC_SWR_D ATA	J1602[14]

Description	Signal	Pin NO	Description	Signal	Pin NO
Speaker amplifier enable 1	SPKR_AMP_ EN1	J1602[15]	Speaker amplifier enable 2	SPKR_AMP_ EN2	J1602[16]
1.8V output power supply	VREG_S4A_ 1P8	J1602[17]	12V output power supply	DC_IN_12V	J1602[18]
5.0V output power supply	MB_VREG_ 5P0	J1602[19]	GND	GND	J1602[20]

3.8.14 On Board PCB WLAN Antenna

The Open-Q 835 carrier board has two on board WLAN PCB antennas that connects to the WiFi / BT on the 835 Processor board via coaxial cables that attaches to MH4L receptacles. These antennas connect to the Processor board in the following configuration:

- WLAN0 on the carrier board connects to ANT0 on the WCN3990 WiFi module
- WLAN1 on the carrier board connects to ANT1 on the WCN3990 WiFi module

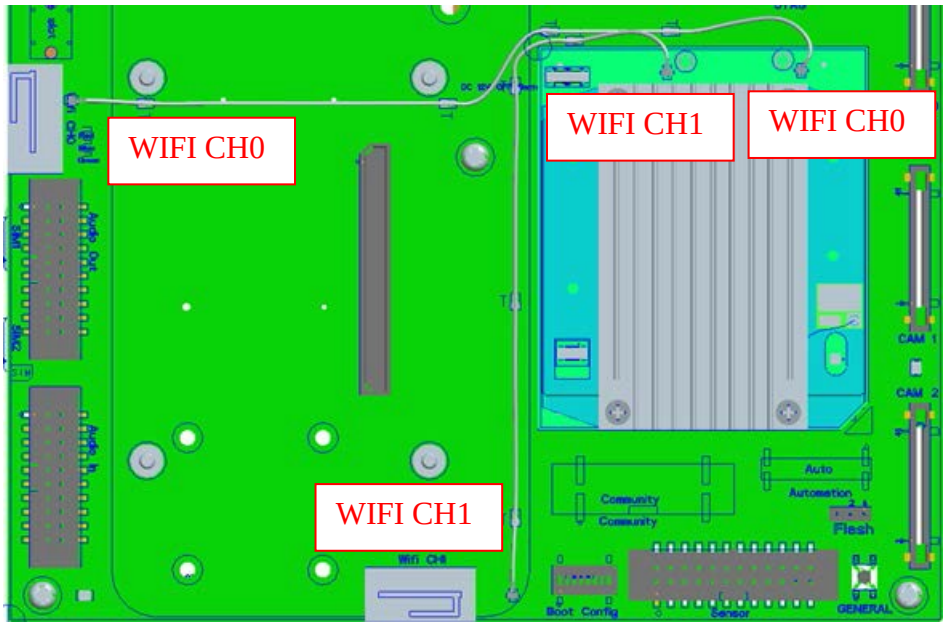

Figure 18 On Board PCB Antennas

3.8.15 On Board PCB GPS Antenna

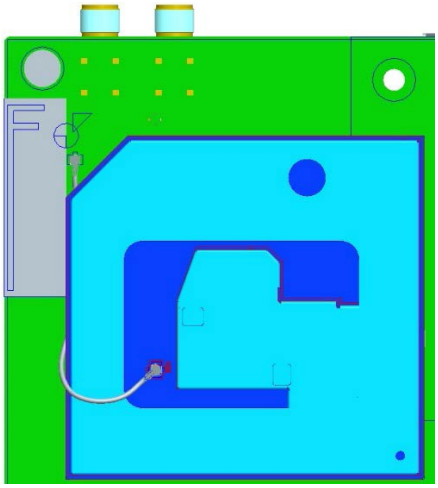

Figure 19 On Board PCB Antennas

The Open-Q 835 carrier board has one on-board PCB antennas on the bottom side that connects to the GNSS card via coaxial cable that attaches to MH4L receptacles. The on-board antenna is connected to the GNSS card by default, meanwhile, there are 0ohm jumpers for user to choose to use external GPS antenna via the SMA connector. The option pads are at the antenna end, before the GPS LNA input. (see table below for details).

Table 3.8-13 GPS Antenna Option

Option	R3804	R3805
On-Board	DNI	Stuff
SMA connector	Stuff	DNI

3.8.16 GPS SMA Connector J3802

The GPS SMA connector is reserved for user to use external antenna. Refer to Table 3.8-13, please stuff R3804 and DNI R3805 to make the path active.

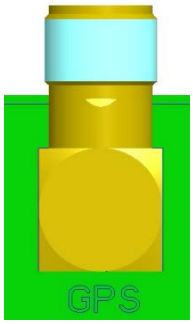

Figure 20 J3802 GPS SMA Connector

If an external GPS antenna is preferred, Intrinsyc recommends the Laird Technologies hepta-band dipole antenna (manufacture part number: MAF94300). It is important to note

that GPS should be used or tested near a window or a location where satellites are easily "seen" by the device.

3.8.17 Open-Q Display

The display output options for the Open-Q 835 Development Kit consists of:

- An HDMI type A connector
  - HDMI 2.0a (4K60) or 4K30 Miracast
- A 100-pin display connector J2 that supports:
  - Dual DSI DPHY 1.2 (up to 3840 x 2400 at 60 fps)
  - Touch screen capacitive panel via I2C or SPI, and interrupts (up to two device)
  - Backlight LED
    - Can support external backlight driver control and power
    - PMI8998 backlight driver supports three LED strings of up to 30mA each with 28V maximum boost voltage

The Open-Q 835 development platform can support the following display combinations:

MIPI DSI	1 x 4lane DSI0 + 1 x 4lane DSI1 1 x 8 lane combining DIS0 and DSI1 for up to 4K resolution 2 x 4-lane DSI DPHY 1.2 and HDMI (4K60) or 4K30 Miracast Display 3840 x 2400 at 60fps, 2560 buffer width (10 layers blending)
HDMI	V2.0 (4K60)

3.8.18 HDMI Connector J1401

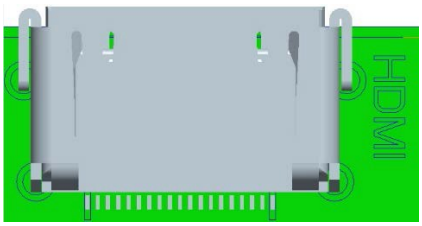

Figure 21 J1401 HDMI Type A Connector

The on board HDMI type A connector enables the Open-Q 835 development platform to connect to an external HDMI monitor/ television via an HDMI cable. As part of a new feature, the APQ8098 can now support up to 4K UHD (3840 x 2400 at 60fps) and HDMI 2.0 (4K60)/ 4K30 Miracast.

Please note that the Open-Q 835 Development Kit is for evaluation purposes only and may not be HDMI compliant.

3.8.19 Display Connector J1301

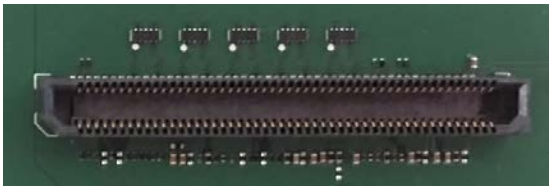

Figure 22 100-Pin Display Connector

The 100-pin display connector provides the following features/ pin-outs that enables the development kit to connect to a MIPI DSI panel/ device:

Note: Please refer to the carrier schematic and display board tech note when designing a custom display board.

- DSI
  - 2 x 4 lane DSI
- Backlight
  - Built-in backlight WLED driver on PMI8998
    - WLED driver supports up to 28.5V output for backlight
  - Primary external backlight (BL0)
    - Backlight control signals
    - External Power
  - Secondary external backlight (BL1)
    - Backlight control signals
    - External power
- Display connector – LCD/ AMOLED
  - PMI8998 programmable display bias output voltage:
    - 5V to 6.1V and -1.4V to -6.0V (LCD display)
    - 4.6V to 5V and -1.4V to -5.4V (AMOLED display)
- Additional GPIOs for general purposes available
- VREG_S4A voltage rail from PM8998
  - Required by display for DOVDD
  - 300mA current path
- Touch Panel

- Supports one touch screen controller
- Supports I2C or SPI via BLSP5 and SSC_2
- Can chose between I2C or SPI signals via MUX

- Power specifications

The display connector supports the following power domains:

Table 3.8-14 Display power Domains

Display Signal	Power Domain
PM8996 LDO22 (3.3-2.8V)	up to 150 mA
PM8996 LDO14 (1.8V- 2.15V)	up to 150 mA
PM8996 LDO15(1.8V – 2.15V)	up to 300 mA
PM8996 S4A (1.8V)	up to 300 mA
Carrier 3.3V	up to 0.5A
Carrier 5 V	up to 1.5A
Carrier 12 V	up to 0.5A

The Intrinsyc AMOLED Display Adapter board (part number: TBD) is an additional PCB that mates with the display connector J1301 on the carrier board. This board allows users to interface with the development kit via the LCD that comes preinstalled on the display board. The following figure illustrates the interfacing connectors on the display board.

Note: The display board comes as an additional add-on to the Open-Q 835 Development Kit. To purchase this, please visit http://shop.intrinsyc.com or contact Intrinsyc at sales@intrinsyc.com for details.

Table 3.8-15 Display Card Mechanical Properties

Dimension	61.48cm^2 (106mm x 58 mm)
Major Interfaces	one 100-pin high speed board-to-board connector

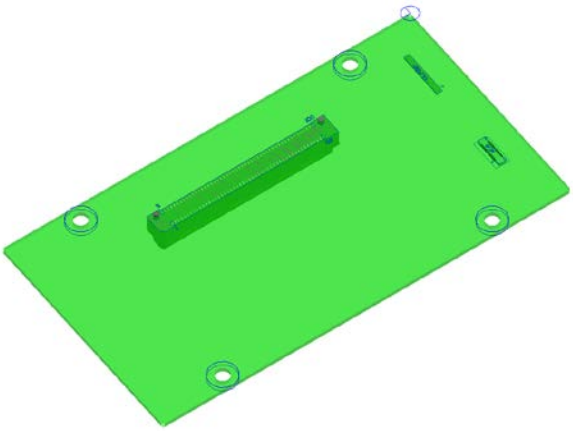

Figure 23 Display Board

3.8.20 Connecting the Display Board to the Development Kit

This configuration allows the user to use the preinstalled LCD display that comes with the display adaptor board. As shown in the block diagram below, the MIPI DSI0 lines, which come from the 100-pin ERM8 connector, directly connects to the LCD panel. See the section below for more details on this LCD panel. It is important to note that connector J0501 on the display board needs to connect to J1301 on the carrier board for this configuration to work.

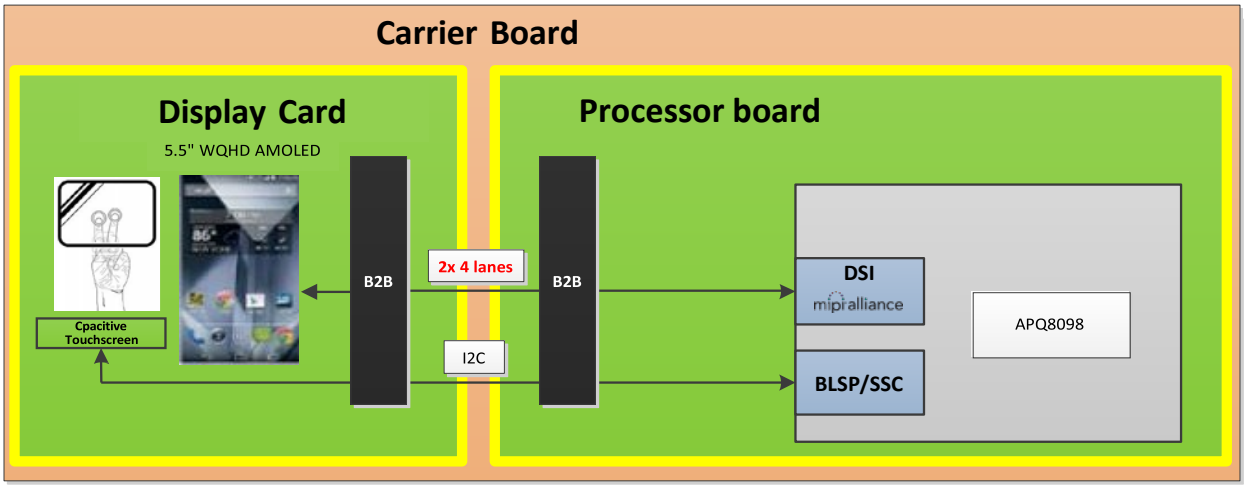

Figure 24 Display Board Default Configuration

3.8.20.1 LCD display panel

The LCD panel comes preinstalled on the Intrinsyc AMOLED display adaptor board. Below are the Panel specifications:

- **Resolution:** 1440x2560
- **LCD Type:** AMOLED
- PCAP touch panel
- **No of Lanes:** 2 x 4 lane MIPI DSI interface via Display Board.
- **Diagonal Length**: 5.5”

Note: **The display above when mounted on the Intrinsyc Open-Q 835 Display Adapter is meant to work with the carrier board. Altering the use of this LCD panel is not recommended.**

3.8.21 Camera Connectors

The Open-Q 835 development kit supports three 4-lane MIPI CSI camera interfaces via three separate JAE 41-pin connectors.

The following are some features of the camera connectors:

- 3 x 4 lane MIPI CSI signals
- Reserved J1702 for integrated flash driver
- Support for 3D camera configuration
    - Separate I2C control (CCI0, CCI1)
- Supports all CSI interfaces
- All camera CSI connectors are on the carrier board edge
- Self-regulated camera modules can be powered with 3.3V power (MB_VREG_3P3)
- Uses JAE FI-RE41S-VF connector for exposing MIPI, CLK, GPIOs and Power rails.
- Please use JAE FI-RE41S-HF to mate with the camera connectors on the carrier board
- The Intrinsyc camera adapter card is designed to be used with the carrier board. Please contact sales@intrinsyc.com for availability

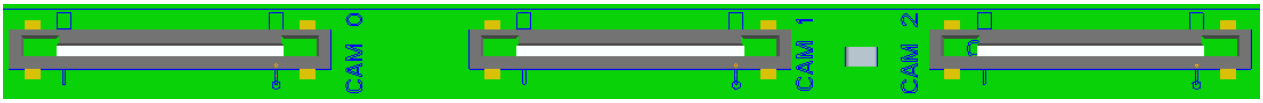

Figure 25 Camera Connectors (J1701, J1801, J1901)

The figure above shows the three MIPI CAM0 (J1701), CAM1 (J1801) and CAM2 (J1901) connectors. The table below outlines the pin outs of these connectors

Table 3.8-16 MIPI CSI Camera Connector Pin out (J1701, J1801, J1901)

Pin#	CAM0 (J1701)	CAM1 (J1801)	CAM2 (J1901)	Description
1, 2, 3	MB_VREG_3P3	MB_VREG_3P3	MB_VREG_3P3	Power output. Connected to main +3.3V MB_VREG_3P3 max current 700mA
4	GND	GND	GND	Ground
5	MB_ELDO_CAM0 _AVDD	MB_ELDO_CAM1 _AVDD	VREG_L22A_2P85	Power output. Connected to external LDO output or PM8998 VREG_L22A regulator. Default MB_ELDO_CAM0_AVDD is 1.8V(DNI R0843 and solder R0844 to set this power rail as +2.8V), MB_ELDO_CAM1_AVDD is +2.8V. Maximum current 300mA
6	MB_ELDO_CAM0 _DVDD	MB_ELDO_CAM1 _DVDD	MB_ELDO_CAM2_DVDD	Power output. Connected to external LDO regulator. Default is +1.2V. Maximum current 500mA
7, 8	MB_ELDO_CAM0 _VCM	MB_ELDO_CAM1 _VCM	MB_ELDO_CAM2_VCM	Power output. Connected to external LDO. Default is +2.8V. Maximum current 300mA
9, 10	VREG_LVS1A_1P 8	VREG_LVS1A_1P 8	VREG_LVS1A_1P 8	Power output. Connected to PM8998 VREG_LVS1A switch output. Default is +1.8V. Maximum current 300mA
11	GND	GND	GND	Ground
12	FLASH_STROBE _EN (APQ_GPIO21)	FLASH_STROBE _EN (APQ_GPIO21)	FLASH_STROBE_ EN (APQ_GPIO21)	Output. Connected to APQ8098 Default use is for camera flash strobe enable
13	CAM0_RST_N (APQ_GPIO30)	CAM1_RST_N (APQ_GPIO28)	CAM2_RST_N (APQ_GPIO9)	Output. Connected to APQ8098 GPIO30 / GPIO28 / GPIO29. Default use is for camera reset
14	CAM0_STANDBY _N (APQ_GPIO29)	CAM1_STANDBY _N (APQ_GPIO27)	CAM2_STANDBY_ N (APQ_GPIO8)	Output. Connected to APQ8098 GPIO29 / GPIO27 / GPIO8. Default use is for camera standby
15	CCI_I2C_SCL0 (APQ_GPIO18)	CCI_I2C_SCL0 (APQ_GPIO18)	CCI_I2C_SCL0 (APQ_GPIO18)	Output. Connected to APQ8098 GPIO18. Default use is for camera CCI0 I2C clock interface
16	CCI_I2C_SDA0 (APQ_GPIO17)	CCI_I2C_SDA0 (APQ_GPIO17)	CCI_I2C_SDA0 (APQ_GPIO17)	Input / output. Connected to APQ8098 GPIO17. Default use is for camera CCI0 I2C data interface
17	CAM_MCLK0_BUF (APQ_GPIO13)	CAM_MCLK1_BUF (APQ_GPIO14)	CAM_MCLK2_BUF (APQ_GPIO15)	Output. Connected to APQ8098 GPIO13 / GPIO14 / GPIO15. Default use is for camera master clock. Maximum 24MHz
18	FLASH_STROBE _TRIG (APQ_GPIO22)	FLASH_STROBE _TRIG (APQ_GPIO22)	FLASH_STROBE_ TRIG (APQ_GPIO22)	Output. Connected to APQ8098 GPIO22. Default use is for camera flash strobe trigger
19	GND	GND	GND	Ground
20	MIPI_CSI0_LANE 0_N	MIPI_CSI1_LANE 0_N	MIPI_CSI2_LANE0 _N	Input. MIPI CSI0 / CSI1 / CSI2 data lane 0

Pin#	CAM0 (J1701)	CAM1 (J1801)	CAM2 (J1901)	Description
21	MIPI_CSI0_LANE 0_P	MIPI_CSI1_LANE 0_P	MIPI_CSI2_LANE0 _P	Input. MIPI CSI0 / CSI1 / CSI2 data lane 0
22	GND	GND	GND	Ground
23	MIPI_CSI0_CLK_ N	MIPI_CSI1_CLK_ N	MIPI_CSI2_CLK_N	Input. MIPI CSI0 / CSI1 / CSI2 clock lane
24	MIPI_CSI0_CLK_ P	MIPI_CSI1_CLK_ P	MIPI_CSI2_CLK_P	Input. MIPI CSI0 / CSI1 / CSI2 clock lane
25	GND	GND	GND	Ground
26	MIPI_CSI0_LANE 1_N	MIPI_CSI1_LANE 1_N	MIPI_CSI2_LANE1 _N	Input. MIPI CSI0 / CSI1 / CSI2 data lane 1
27	MIPI_CSI0_LANE 1_P	MIPI_CSI1_LANE 1_P	MIPI_CSI2_LANE1 _P	Input. MIPI CSI0 / CSI1 / CSI2 data lane 1
28	GND	GND	GND	Ground
29	MIPI_CSI0_LANE 2_N	MIPI_CSI1_LANE 2_N	MIPI_CSI2_LANE2 _N	Input. MIPI CSI0 / CSI1 / CSI2 data lane 2
30	MIPI_CSI0_LANE 2_P	MIPI_CSI1_LANE 2_P	MIPI_CSI2_LANE2 _P	Input. MIPI CSI0 / CSI1 / CSI2 data lane 2
31	GND	GND	GND	Ground
32	MIPI_CSI0_LANE 3_P	MIPI_CSI1_LANE 3_P	MIPI_CSI2_LANE3 _P	Input. MIPI CSI0 / CSI1 / CSI2 data lane 3
33	MIPI_CSI0_LANE 3_N	MIPI_CSI1_LANE 3_N	MIPI_CSI2_LANE3 _N	Input. MIPI CSI0 / CSI1 / CSI2 data lane 3
34	GND	GND	GND	Ground
35	CCI_I2C_SDA1 (APQ_GPIO19)	CCI_I2C_SDA1 (APQ_GPIO19)	CCI_I2C_SDA1 (APQ_GPIO19)	Output / Input. Connected to APQ8098 GPIO19. Default use is for camera CCI1 I2C data interface
36	CCI_I2C_SCL1 (APQ_GPIO20)	CCI_I2C_SCL1 (APQ_GPIO20)	CCI_I2C_SCL1 (APQ_GPIO20)	Output. Connected to APQ8098 GPIO20. Default use is for camera CCI1 I2C clock interface
37	CAM_IRQ (APQ_GPIO26)	CAM_IRQ (APQ_GPIO26)	CAM_IRQ (APQ_GPIO26)	Input. Connected to APQ8098 GPIO26. CAM_IRQ signal
38	CAM0_MCLK3 (APQ_GPIO16)	CAM1_MCLK3 (APQ_GPIO16)	CAM2_MCLK3 (APQ_GPIO16)	Output. Connected to APQ8098 GPIO16. Default use is for camera master clock. Maximum 24MHz
39	MB_ELDO_CAM0 _DVDD	MB_ELDO_CAM1 _DVDD	MB_ELDO_CAM2_DVDD	Power output. Connected to external LDO regulator. Default is +1.2V. Maximum current 500mA
40, 41	MB_VREG_5P0	MB_VREG_5P0	MB_VREG_5P0	Power output. 5V Power supply. Maximum 700mA

Note: A connection from the camera connectors on the carrier board to the Intrinsyc camera adapter board is established by a 41-pin cable assembly from JAE Electronics (part number JF08R0R041020MA)

The following table shows the combinations of camera usage for different use cases

Table 3.8-17 MIPI CSI Camera Use Cases

CSI PHY	Use case	Comment
CSI0	Up to 4 lane	One Camera of 4 lane or One camera of 3 lane One Camera of 2 lane One Camera of 1 lane
CSI 1	Up to 4 lane	One Camera of 4 lane or One camera of 3 lane One Camera of 2 lane One Camera of 1 lane
CSI 2	Up to 4 lane	One Camera of 4 lane or 2 x Camera of 1 lane each
CSI0 + CSI1	Up to 4 lane 3D	4 lane 3D use case / Dual 4 lane configuration
CSI 2	Up to 1 lane 3D	1 lane 3D use case / Dual 1 lane configuration
CSI0 + CSI1 + CSI2	Up to 4 lane	Three 4-lane CSI (4+4+4 or 4+4+2+1)
CPHY		Three 3-trio CPHY1.0

3.8.22 USB 3.1 TYPEC connector J1101

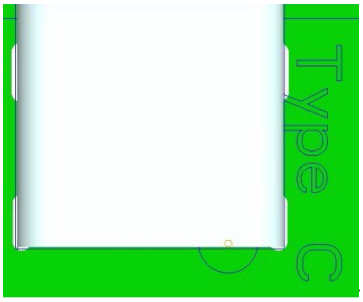

Figure 26 J1101 USB3.1 TYPE-C

The on board Type-C connector J1101 supports USB 3.1 Gen1, which also supports Type-C with DisplayPort V1.3

3.8.23 GNSS Card

Table 3.8-18 Open-Q 835 GNSS Card Mechanical Properties

Dimensions	32.36cm^2 (58.3mm x 55.5mm)
Major Interfaces	two 240-pin high speed board-to-board connector

WTR5975: GNSS Front End WTR5975 is the primary GNSS radio interface used on the HDK835 development kit. This provides the RF capabilities for GNSS functions. It has

both digital and RF interfaces. Digital interface is required for configuration and status for the APQ8098 processor.

The following are the operating frequencies for WTR5975

GPS: 1574.42 MHz – 1576.42 MHz

GLONASS: 1598 MHz to 1606 MHz

COMPASS: 1559.05 to 1563.14MHz

Galilei: 4.092MHz BW (centered on 1575.42MHz)

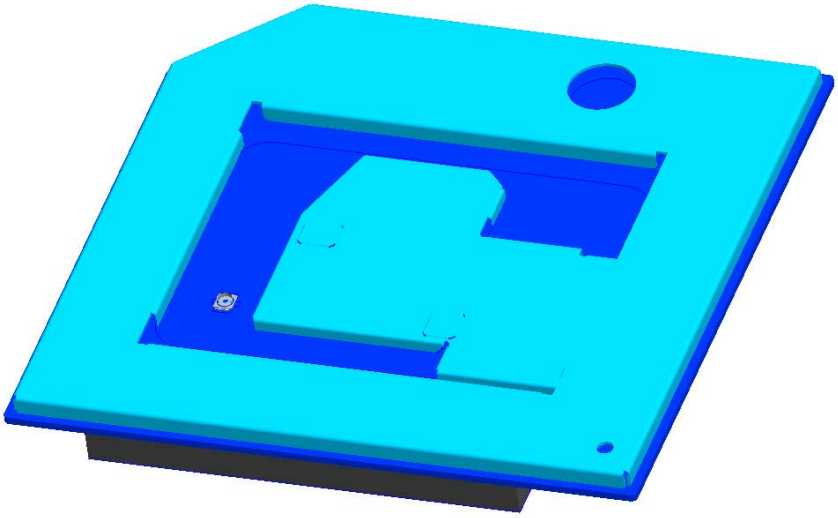

Figure 27 Open-Q 835 GNSS Card

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